

Ansys HFSS: Layout Driven Assembly in Ansys Electronics Desktop

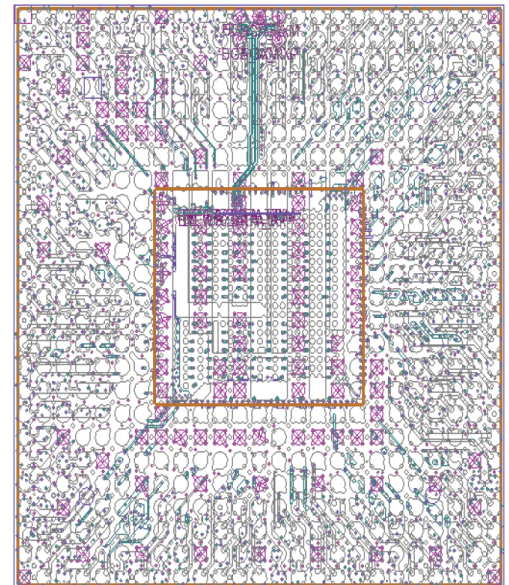
The Ansys Electronics Desktop (AEDT) is an integrated environment with an easy-to-use interface that provides a streamlined workflow between Ansys EM field solvers, circuit/system simulators, ECAD links and MCAD connector models. It now allows users to import mechanical CAD connector models to be placed in the layout environment with boards and packages. This gives engineers the ability to set up connector/package/board models in one environment, choose the solver technology that is best for each simulation, and then perform 3D Extractions on the concatenated models.

/ Introduction

In today's design flow for signal integrity applications, there are two separate procedures: extraction and circuit simulation. For the extraction process, typically, customers are using Ansys Electromagnetic tools to solve for high frequency S-parameter data from their connectors, packages and board designs. Once they perform the S-parameter extraction, they import those models into a circuit simulator to wire them up together. Using net listing is time-consuming, but even using a schematic interface to wire up black boxes can be very tedious and error prone. The new capability in HFSS 3D Layout allows users to graphically connect their EM models to perform 3D extraction, transient circuit analysis and linear network analysis (LNA) simulations. This paradigm shift in the design flow allows users to pick and place 3D CAD models onto a PCB, choose the appropriate solver technology for the extraction, and perform 3D electromagnetic extraction, transient circuit analyses and LNA frequency sweeps, all in one interface, without having to create a circuit schematic.

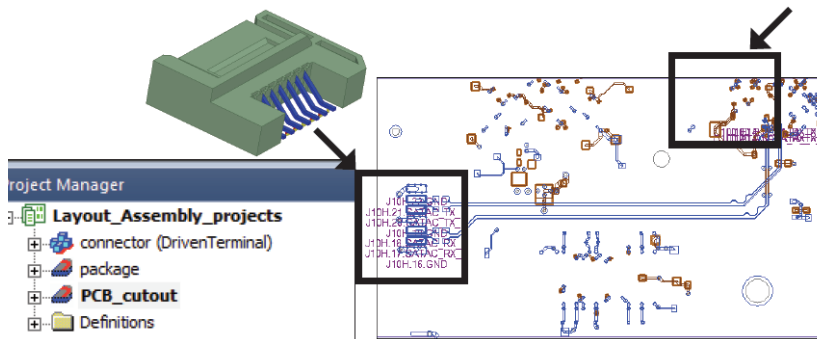
/ Key Benefits

- Assembly of a complete system can be performed in the 3D Layout GUI.
- Creation of schematics is not needed for transient circuit analysis or LNA simulations.
- Access to HFSS and SIwave SYZ solvers is available for the Layout models.
 - Variables can be added to the geometry easily within the 3D Layout GUI, and the HFSS and/or SIwave SYZ solver can then run the parametric variations.
 - Hybrid technology enables fast turnaround on iterations.
 - FEM provides validation.



Layout Driven Assembly

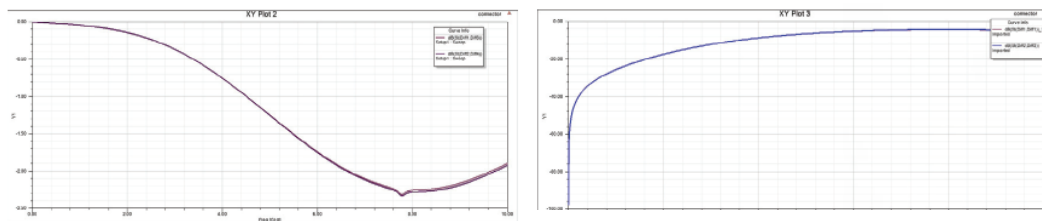
The end goal of this example is to run a transient circuit analysis or LNA simulation on an assembled geometry that includes a connector, a cutout section of a PCB and a package model. The nets of interest are two 6 Gb/s SATA differential pairs.



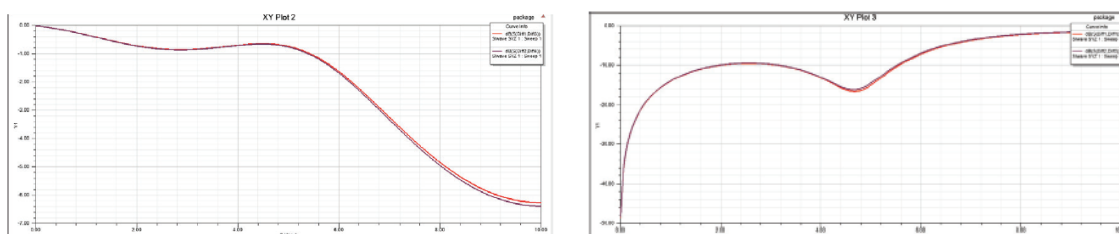
Open the project named **Layout_Assembly_projects.aedt**. This project contains three models: one HFSS 3D model of a connector, one HFSS 3D Layout project of a package design with two differential pairs of nets and one HFSS 3D Layout project of a section of a board with two differential pairs of nets.

Expand each of the of the design projects and view the differentials-parameter results for the solved nets.

- Connector - HFSS 3D design.
 - Use the HFSS 3D FEM solver.
 - Solution Frequency: 5 GHz.
 - Frequency Sweep: 0-10 GHz.

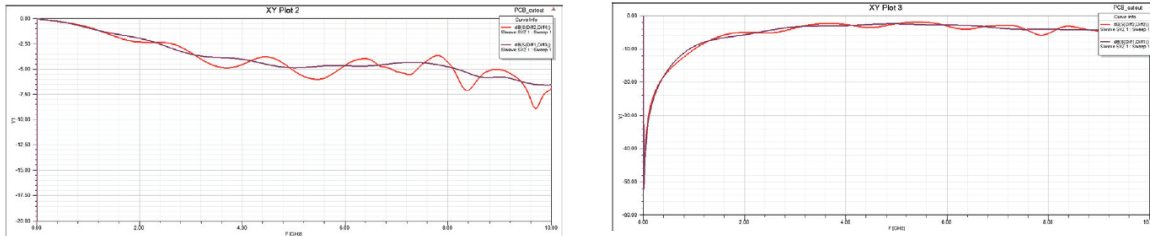


- Package – HFSS 3D Layout design.
 - Use the Siwave SYZ solver.
 - Frequency Sweep: 0-10 GHz.
- PCB_cutout – HFSS 3D Layout design.
 - Use the Siwave SYZ solver.
 - Frequency Sweep: 0-10 GHz.

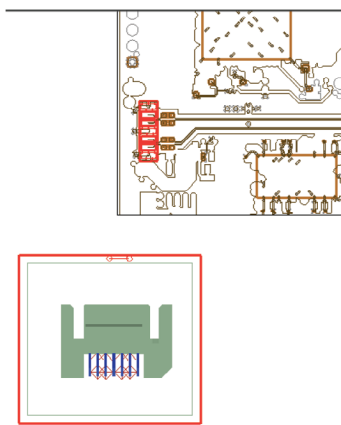
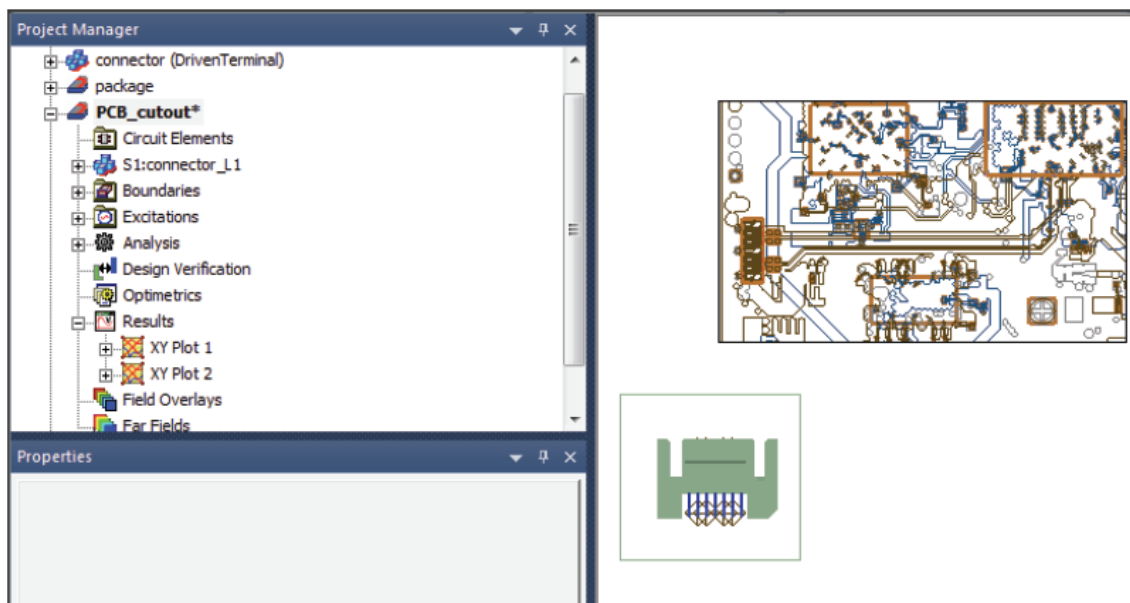


Place Connector onto the Board

To place the connector onto the board, left click the connector design, then drag and drop it into the PCB_cutout 3D Layout design. The connector design will appear in the PCB_cutout design as a subcircuit. It places the 3D component in the Layout design in an arbitrary location.




To place the connector in the right location, which is on top of the J10H footprint, first highlight the 3D component to bring up its properties. In the Param Values tab, uncheck HFSS Mesh (Beta). The HFSS Mesh Beta feature enables 3D HFSS FEM extraction of the Connector plus the PCB. Next, click the Footprint tab, then place a checkmark next to 3D Placement. Then, multiselect the 3D connector component and the J10H footprint.

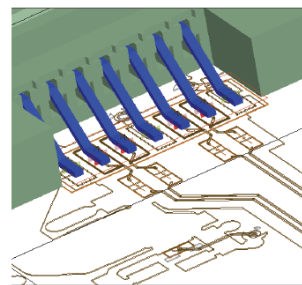
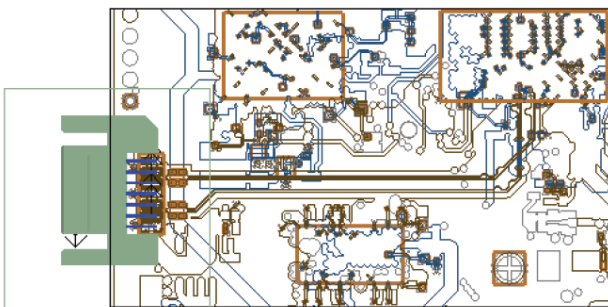
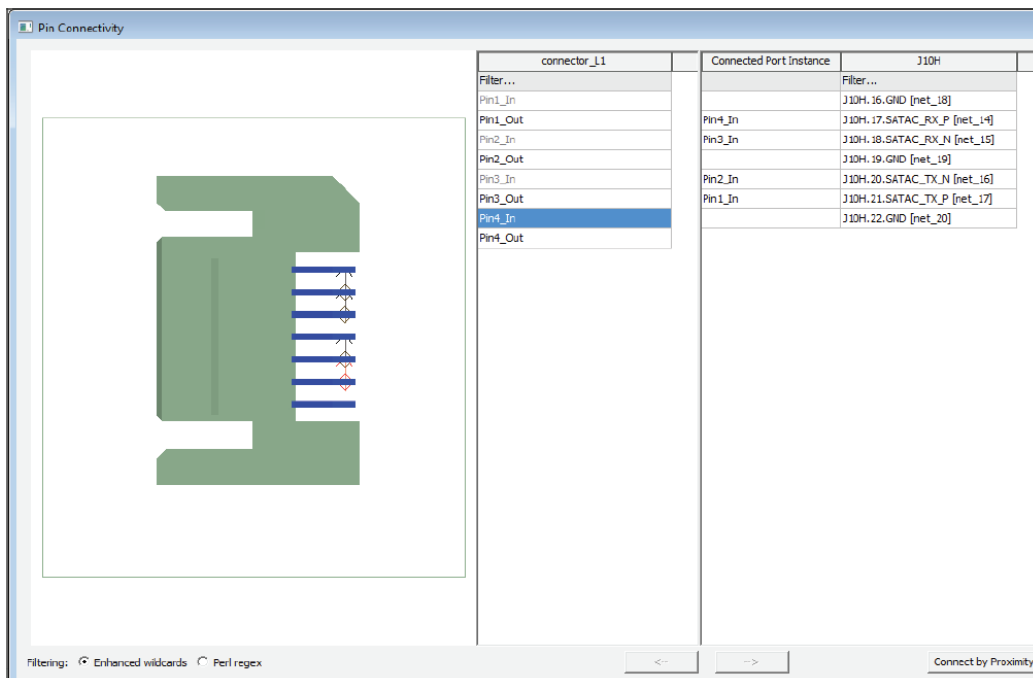
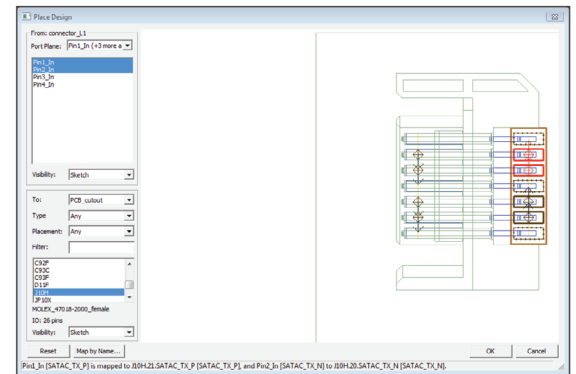


Click **Layout -> Place Design**. Multi-select Pin1_In and Pin2_In (in that order). For the PCB_cutout design, change the 'Visibility' to 'Sketch.' Move the cursor to find the pin named J10H.21.SATAC_TX_P. Left click that pin. Next, move the cursor down to find the pin named J10H.21.SATAC_TX_N. Left click that pin. The model will then snap into place. The bottom of the Place Design pop-up window will tell you the pin associations. Click OK when done.

/ Place Package onto the Board

The next screen that appears is the Pin Connectivity window. window is connecting the ports from the connector to the ports of the board file. Select Pin1_In from the connector_L1 column. Select J10H.21.SATAC_TX_P [SATAC_TX_P] from the J10H column. Select the right arrow button  to associate the pins. Repeat this process for the next three pin associations:

- Pin Connectivity window
 - **Pin1_In → J10H.21.SATAC_TX_P [SATAC_TX_P]**
 - **Pin2_In → J10H.20.SATAC_TX_N [SATAC_TX_N]**
 - **Pin3_In → J10H.18.SATAC_RX_N [SATAC_RX_N]**
 - **Pin4_In → J10H.17.SATAC_RX_P [SATAC_RX_P]**
 - Click OK when done




/ Place Package onto the Board

To place the package onto the board, left click the package design, and drag and drop it into the PCB_cutout 3D Layout design. When the Paste Design Options window pops up, choose Link to Original. The package design will appear in the PCB_cutout design as a sub-circuit. It places the 3D component in the Layout design in an arbitrary location. To place the package in the right location, which is on top of the U100 footprint, first highlight the 3D component to bring up its properties.

- In the Properties window
 - In the Param Values tab, uncheck HFSS Mesh (Beta)
 - Click the Footprint tab, then place a checkmark next to 3D Placement
 - Change Rotation Axis to Z
 - Change Rotation Angle to 180

Next, in the GUI, multi-select the package component and the U100 footprint.

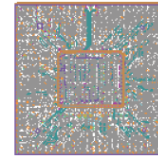
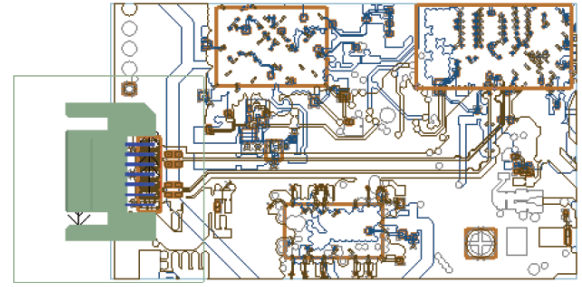
Click Layout > Place Design. In the Place Design window, click Map By Name ... Highlight BGA.A12.SATA_TXP[SATA_TXP], then BGA.A14.SATA_RXM[SATA_RXM] (in that order) in the From column. Next, highlight U100.A12.SATA_TX_P[SATA_TX_P] and U100.A14.SATA_RX_N[SATA_RX_N] (in that order).

Click OK to map the pins. Click OK to close the Place Design window. The next screen that appears is the Pin Connectivity window. This window is connecting the ports from the package to the ports of the board file. Select BGA.A12.SATA_TXP from the package column. Select U100.A12.SATA_TX_P[SATA_TX_P] from the U100 column. Select the right  arrow button to associate the pins.

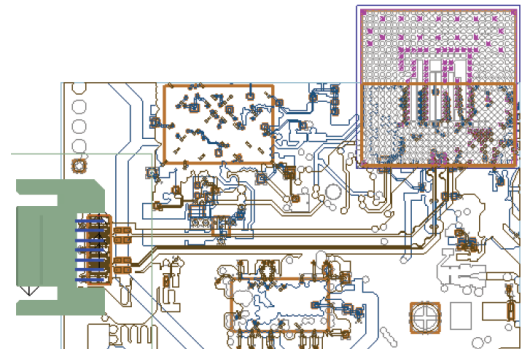
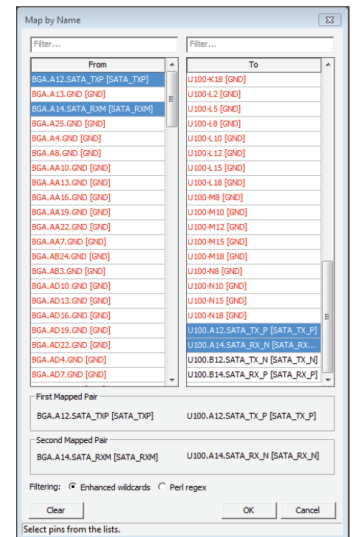
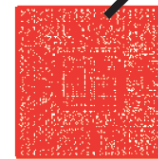
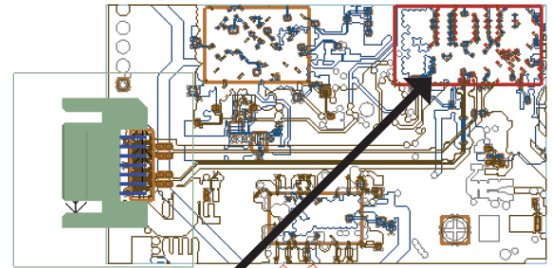
Connect the remaining 3 pins as defined below:

- Pin Connectivity window
 - BGA.A12.SATA_TXP → U100.A12.SATA_TX_P[SATA_TX_P]
 - BGA.A14.SATA_RXM → U100.A14.SATA_RX_N[SATA_RX_N]
 - BGA.A12.SATA_TXM → U100.B12.SATA_TX_N[SATA_TX_N]
 - BGA.A14.SATA_RXP → U100.B14.SATA_RX_P[SATA_RX_P]
 - Click OK to map the ports

Make sure that both 3D Components have the HFSS Mesh unchecked.



U1 package



/ Define Interface Ports on the Connector and Package

To place Interface ports on the connector in order to run the LNA, right click on the connector, click Port → Interface Ports → Add Interface Ports at Unconnected Pins.

To place Interface ports on the BGA in order to run the LNA, right click on the connector, click Port → Interface Ports → Add Interface Ports at Unconnected Pins.

/ Define Solver Settings

To add an LNA analysis type, click HFSS 3D Layout → Solution Setup → Add Nexxim Solution Setup → Linear Network Analysis. Edit the sweep:

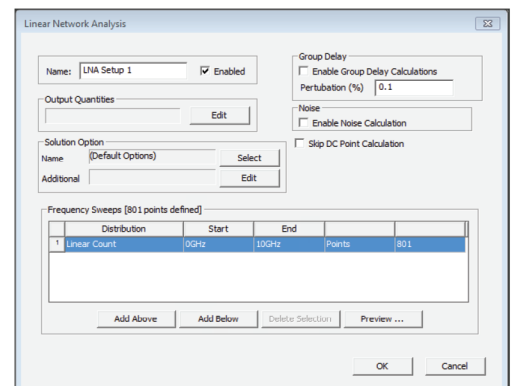
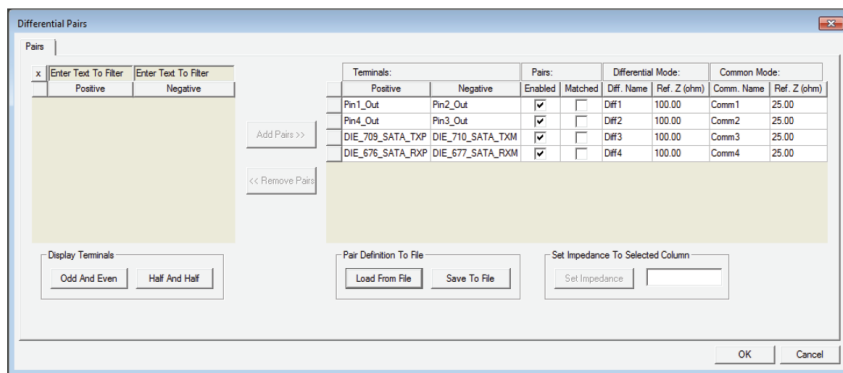
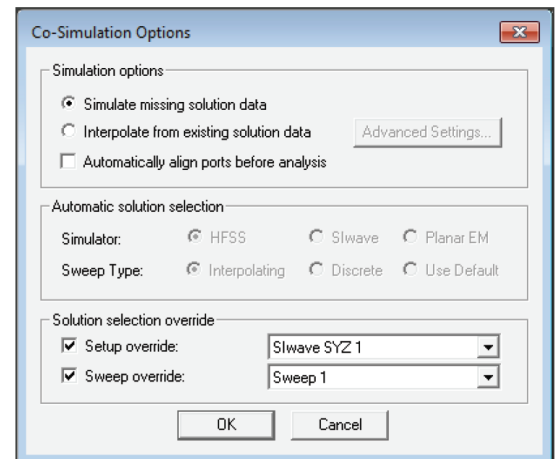
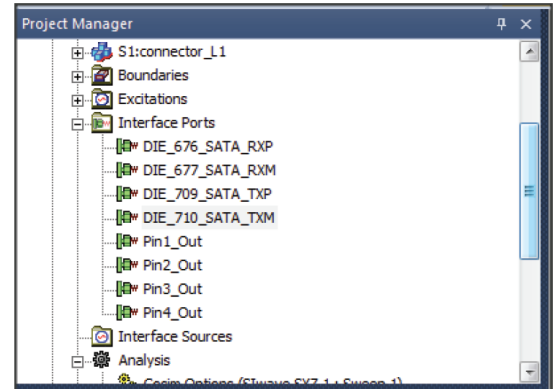
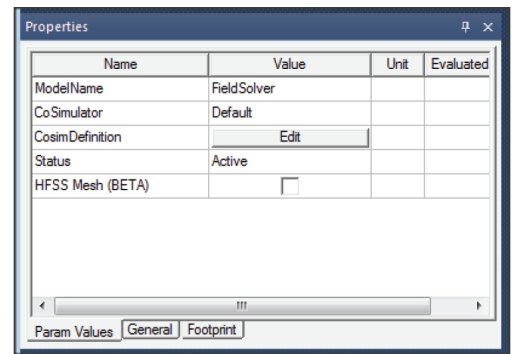
- Linear Count
- Start: 0Hz
- End: 10 GHz
- Points: 801
- Click OK to exit

To allow the LNA to use the existing SIwave solutions, right click on Cosim Options → Properties. Place a checkmark in Setup override. Also, place a checkmark in Sweep override. Click OK to exit.

To run the analysis, right click on LNA Setup 1 and click Analyze. To view the Differential Insertion and Return Loss, right click Interface Ports in the Project Manager. Next, click Differential Pairs. Arrange the ports in the configuration below:

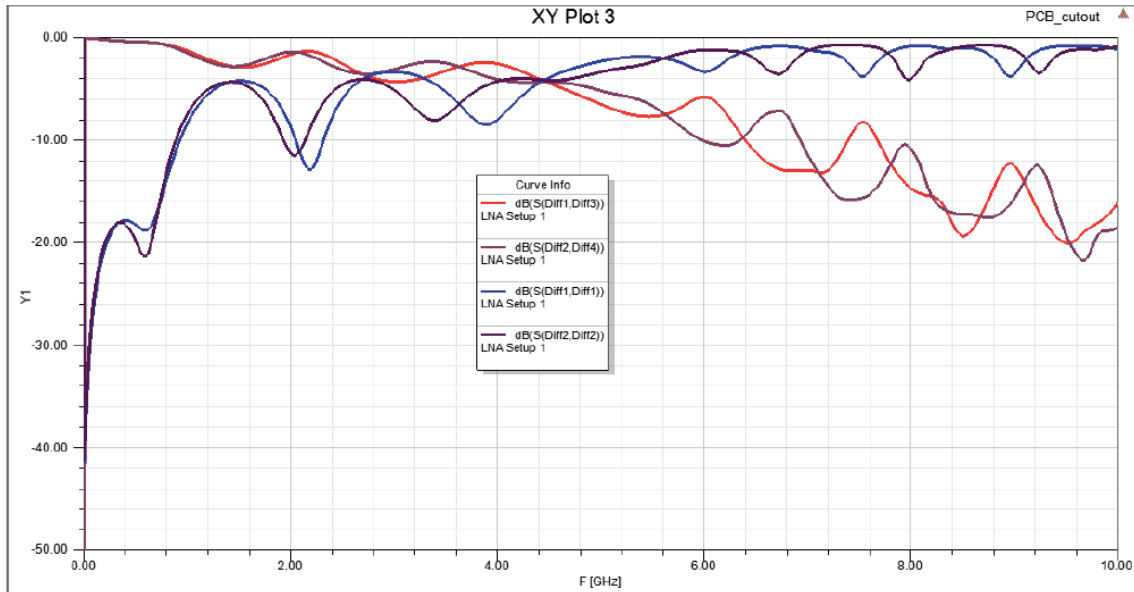
To view the S-parameter results of differential IL and differential RL, right click on Create Standard Report → Rectangular Plot. Under Context, change the Solution to be LNA Setup 1. For Show, choose Differential Pairs. Plot the following:

- S parameter.
 - $\text{dB}(S(\text{Diff1}, \text{Diff3}))$
 - $\text{dB}(S(\text{Diff2}, \text{Diff4}))$
 - $\text{dB}(S(\text{Diff1}, \text{Diff1}))$
 - $\text{dB}(S(\text{Diff2}, \text{Diff2}))$



Summary

The new capabilities in HFSS 3D Layout deliver powerful capabilities to assemble an electronic system with IC packages, sockets, printed circuit boards and connectors, and then perform electromagnetic field simulation plus transient circuit analysis of that system automatically. This allows leading companies to break through the established silos of separate IC, package and board design, and gain insight to the integrated IC-package-board design.



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