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PREDICTING FATIGUE OF SOLDER JOINTS SUBJECTED TO HIGH NUMBER OF POWER CYCLES

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Solder joint reliability of surface mount technology (SMT) components connected to printed circuit boards is well-documented. However, much of the testing and data is related to high-strain energy thermal cycling experiments relevant to product qualification testing (i.e, -55 °C to 125 °C). Relatively little information is available on low-strain, high-cycle fatigue behavior of solder joints, even though this is increasingly common in a number of applications due to energy savings sleep mode, high variation in bandwidth usage and computational requirements, and normal operational profiles in a number of power supply applications.

In this paper, 2512 chip resistors were subjected to high (>50,000) number of short duration (<10 min) power cycles. Environmental conditions and relevant material properties were documented and the information was inputted into a number of published solder joint fatigue models. The requirements of each model, its approach (crack growth or damage accumulation) and its relevance to high cycle fatigue are discussed. Predicted cycles to failure are compared to test results as well as warranty information from fielded product. Failure modes were confirmed through cross-sectioning. Results were used to evaluate if failures during accelerated reliability testing indicate a high risk of failures to units in the field. Potential design changes were evaluated to quantify the change in expected life of the solder joint.

/ SOLDER JOINT FATIGUE PREDICTION - THEORY

Degradation of solder joints due to differential expansion and contraction of joined materials has been a known issue in the electronics industry[1] since the basic construction of modern electronic design was finalized in the late 1950s early 1960s. Initial assessment of the behavior borrowed heavily from observation of structural materials in the early 1950s, such as solder fatigue in automotive radiators[2] and thermal fatigue of steels.[3-5] The resulting Coffin-Manson relation states that the number of cycles to failure has a power law dependence on the magnitude of the plastic strain, or inelastic deformation, experienced during that specific thermal cycle.

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\varepsilon_f}\right)^c$$

Where ε_f, and c are empirically derived constants. This approach provided a predictive model for low-cycle (< 10,000 cycles) fatigue behavior and, in combination with the Basquin equation for high-cycle (> 100,000 cycles) fatigue, resulted in a uniform approach for fatigue prediction across a wide range of use conditions as seen in Figure 1.
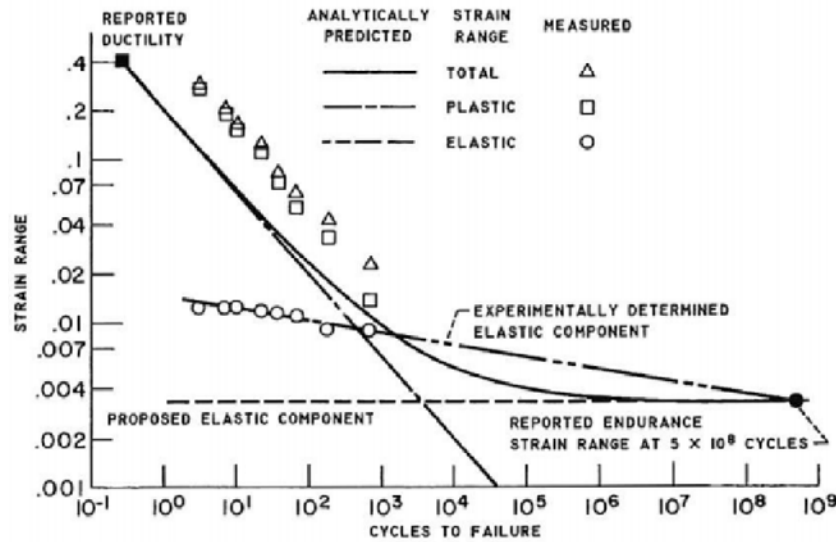
Figure 1. Fatigue curve of 24ST aluminum, showing low cycle and high cycle fatigue[6]

While the Coffin-Manson equation was based on a sound understanding of material science and mechanics, it was difficult to implement for applications relevant to electronics packaging. Solder, the key interconnect material at risk of thermomechanical fatigue in electronic packaging, was applied in volumes too small to directly measure plastic strain and in geometries too complicated to solve through simple mechanics models (Coffin and Manson's original papers used flat plate geometries as an example).

Norris and Landzberg[7] attempted to address these deficiencies by proposing that plastic strain dominated thermomechanical fatigue of eutectic SnPb alloy, the primary solder of choice in electronic packaging at that time. In ignoring the influence of elastic strain, Norris-Landzberg were able to draw a direct relationship between change in temperature and plastic strain. To account for the influence of creep-driven plasticity, a mechanism of less concern for high temperature steels, Norris- Landzberg added additional correction factors based on cyclic frequency (which is directly related to dwell times) and maximum temperature.

$$AF = \left(\frac{\Delta T_A}{\Delta T_B}\right)^{1.9} \left(\frac{f_B}{f_A}\right)^{1/3} exp\left(\frac{E_a}{k}\left[\frac{1}{T_B} - \frac{1}{T_A}\right]\right)$$

This approach to predicting solder joint lifetime under thermal cycling was widely embraced by the electronics community, to the extent that the Norris-Landzberg equation is the only technique referenced in the relevant JEDEC qualification documents, JESD47[8] and JESD94.[9]

The Norris-Landzberg equation, while eminently practical, has several key limitations. The most critical is the inability to make a fatigue prediction without test data. This effectively eliminates the use of Norris-Landzberg from any design activities. The equation is also based on the assumption that creep behavior is driven exclusively by temperature and time, whereas there is a critical applied stress element. Depending upon the packaging architecture, the change in applied stress at different thermal cycles could have a more substantive effect then identified through frequency and temperature, possibly changing rate constants depending on the solder joint configuration and overall packaging architecture.[10] Finally, the equation is dependent upon the plastic strain being driven by the same mechanism in both environments. As demonstrated by deformation maps (Figure 2), different atomic-level mechanisms can be triggered to induce plasticity and creep behaviors depending on the specific combination of temperature and applied stress. The limitation of this approach has been made most obvious by the inability to develop a Norris-Landzberg equivalent for Pb-free solders (SAC305).[11-12]
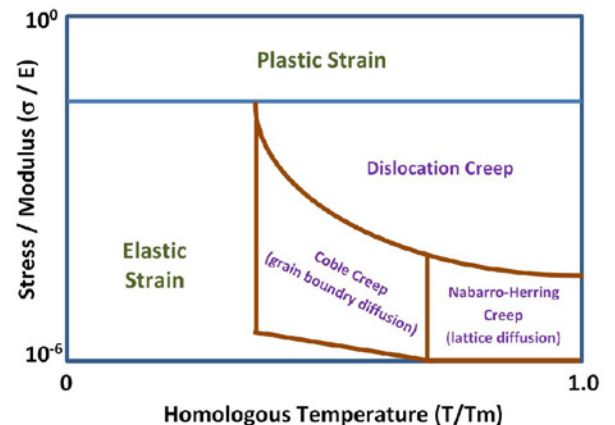

Figure 2. A representative schematic of a deformation map showing the various mechanisms that can induce damage during cyclic fatigue.

Further improvement to the prediction of solder fatigue was provided by Engelmaier,[13] who returned back to the principles of Coffin Manson, but used solid mechanics models more relevant to the solder joint geometry and low-cycle fatigue data for SnPb solder.[14] To determine the plastic strain, or strain range, Engelmaier assumed that the in-plane (shear) steady-state strains dominated low-cycle fatigue behavior. This allowed for the use of a distance-to-neutral model.

$$\Delta\gamma = C\frac{L_D}{h_s}\Delta\alpha\Delta T$$

With C being a geometry-dependent constant ($1/\sqrt{2}$ for leadless ceramic chip carriers), L_D is the diagonal distance from the neutral point (assumes a square/rectangle shape), $\Delta\alpha$ is the difference in thermal expansion between the die/component and substrate/printed board, and ΔT is the thermal cycle. Engelmaier then derived ε_f and c through curve fitting of the Wild data, with where Ts is the average temperature during the thermal cycle and f is the frequency of the thermal cycle.

$$\varepsilon_f = 0.325 \text{ and}$$

$$c = (-0.442) - (6x10^{-4}\, T_s) + (1.74x10^{-2})[\ln{(1+f)}]$$

In some respects, the Engelmaier model was even more successful than the Norris-Landzberg. Like Norris-Landzberg, the inputs required to use the Engelmaier model was available to the practicing engineer. It was also widely adopted in the industry, primarily through IPC SM-785.[15] The Engelmaier overcame some of the limitations of the Norris-Landzberg, including a strong link to the original Coffin-Manson methodology, ability to predict fatigue performance without testing, consideration of the package geometry, and a basis in experimental fatigue results.

The Engelmaier approach, while superior to previous attempts to predict low-cycle solder fatigue both in accuracy and practicality, had some limitations. One of the flaws of the Engelmaier approach lies with the Wild data that is the basis of its fatigue exponent. Wild performed isothermal mechanical fatigue experiments at 25 °C and 100 °C at between 4 and 300 cycles per hour. These temperature ranges are above room temperature and therefore provide limited insight into fatigue behavior at colder temperatures where creep-based mechanisms are reduced and plasticity-driven mechanisms play a larger role in fatigue behavior. The cyclic frequency is higher than most thermal cycling test conditions, which are typically one (1) to two (2) per hour, and far higher than field conditions, which can require several hours to go through a thermal cycle. This has the effect of minimizing the time dependency of creep mechanisms and the resulting damage evolution. This tendency to overestimate and underestimate creep effects may have contributed to the accuracy of the predictions.

An additional challenge to both Coffin-Manson and the derived Engelmaier model was their assumption that the plastic strain was constant over the entire temperature cycle. Work by Hall measured a hysteresis loop, where the stress-strain relationship could vary dramatically as the solder joint was exposed to a range of temperatures (see Figure 3).[16] It is important to note that the nominal shape of hysteresis loops can be more uniform, depending upon the applied stress, temperature, and dwell time. The cycle measured by Hall induced failure in less than 500 cycles, which is typically too low to be accurately predicted through analytical means).

Additional experiments also demonstrated a more consistent correlation between strain energy and cycles to failure with fewer dependencies on geometry or load orientation.[17] These observed behaviors necessitated a move to a strain energy based prediction scheme. Blattau introduced a modification of the Engelmaier model that replaced strain range with strain energy.[18]
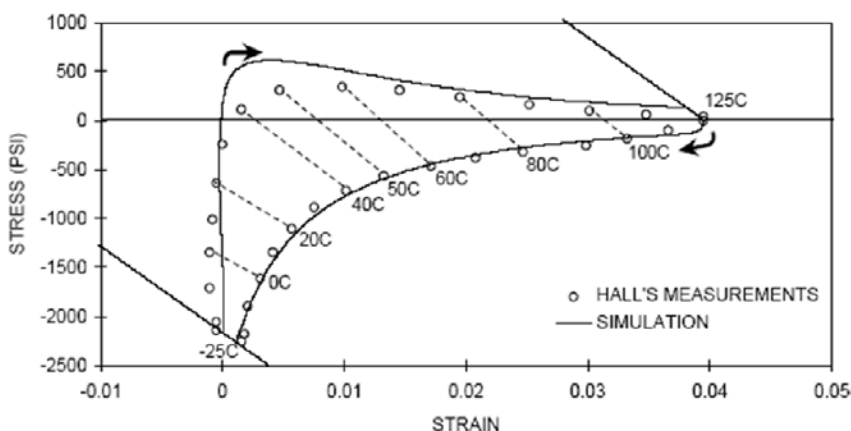

Figure 3. Hysteresis loop of a leadless ceramic chip carrier solder joint during thermal cycling between -25° C and 125° C

To compute strain energy, Blattau used a foundation stiffness model to calculate the force being applied to the solder joint based on displacement equations,

$$\alpha_1 - \alpha_2 * \Delta T * L_D = F\left(\frac{L_D}{E_1 A_1} + \frac{L_D}{E_2 A_2} + \frac{h_s}{A_s G_s} + \frac{h_c}{A_c G_c} + \left(\frac{2-\upsilon}{9G_b a}\right)\right)$$

where L_D is the diagonal length (distance to neutral point), E is the elastic modulus, A is the area, h is the thickness, G is the shear modulus, a is the edge length of the bond pad, 1 refers to the component, 2 refers to the board, s refers to the solder joint, c refers to the bond pad, and b refers to the board. The shear stress can then be computed by dividing the force by the effective solder joint area.

Once the strain range and the shear stress are computed, the strain energy is calculated assuming a hysteresis loop that is roughly equilateral in shape (Figure 4).
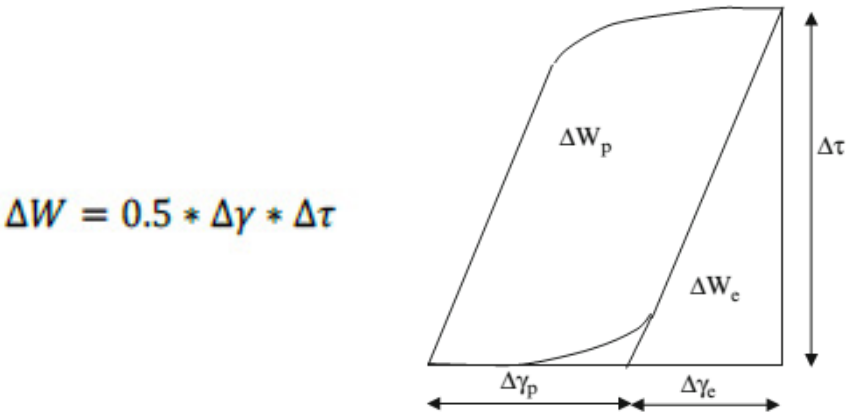

$$\Delta W = 0.5 * \Delta\gamma * \Delta\tau$$

Figure 4: Representative schematic of a solder joint hysteresis loop[19].

The relationship between cycles to failure and strain energy is then determined based on work performed by Syed,[20] who demonstrated a power law correlation between strain energy and cycles to failure with an exponent of -1. The foundation of this behavior is based on first principles of secondary creep behavior. The Blattau approach, which combines the first-order equations derived from the original Coffin-Manson equation with the observed dependence on strain energy, has been validated for both chip components and ball grid array packaging technology (see Figure 5).
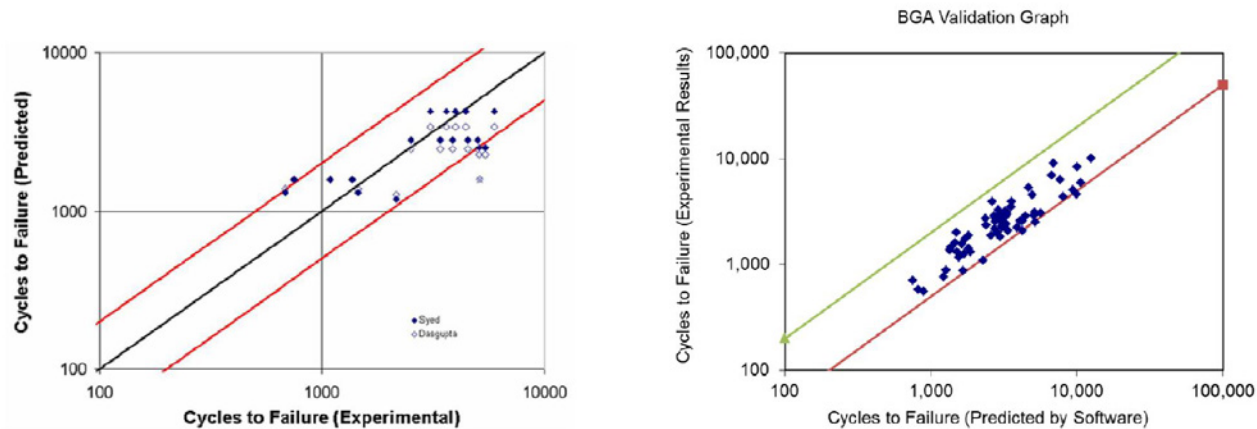

Figure 5. Validation graphs for chip components and ball grid array (BGA) packaging technology

/ SOLDER JOINT PREDICTION – VALIDATION (POWER CYCLING)

Almost all solder prediction models go through a validation process where predictions are compared to experimental results. These validation processes can be a direct comparison of measured time to failure to theoretical predictions or the experimental results can be correlated to normalized parameters relevant to the model algorithm. Most validation activities attempt to provide a correlation over three orders of magnitude, typically between 100 to 10,000 cycles.

Isothermal testing tends to be the dominant vehicle for validation studies. A study by the University of Maryland determined that over 82% of the test conditions reported in the IEEE literature were isothermal thermal cycles.[21] This is true even though one of the initial concerns regarding solder joint fatigue was the performance of devices subjected to power cycling. The majority of publications on solder fatigue under power cycling focus on the die attach structure common within high power insulated gate bipolar transistors (IGBT).[22, 23] This specific structure does not necessarily lend itself to common surface mount (SMT) solder joints due to the highly constrained layer architecture and the inability to directly monitor or define die attach failure.

The limited studies on power cycling of standard surface mount devices have primarily focused on correlation to isothermal cycling or shock. An earlier paper by Popps et. al. showed a 50% increase in lifetime with power cycling, even though the power cycle had a longer dwell time (15 minutes vs. 5 minutes) and a faster ramp rate (60 °C/min vs. 20 °C/min).[24] A similar increase in number of cycles to failure was predicted and observed by Li et. al.;[25] they assigned this difference in behavior to the large thermal gradient across the BGA package, which effectively increased the coefficient of thermal expansion (CTE) of the BGA under the die shadow while limiting the degree of expansion over the diagonal length.

The limiting factor of these papers and other investigations on power cycling of SMT packages is that the time is typically less than 10,000 cycles. While this cycle count could be considered as the outer bound of low cycle fatigue (others believe plastic strain is dominant out to 100,000 cycles), it fails to consider that an increasing number of applications are expected to have tens of thousands of power cycles in the actual field application. Enterprise applications are increasingly powering down, either to sleep mode or turn off, to save energy. To conserve battery charge, consumer mobile devices (smart phones, tablets, and laptops) can experience between 10 to 50 power cycles per day for three to five years, which can result in a total of 15,000 to 90,000 power cycles over its lifetime. A similar environmental profile is starting to ramp up in automotive applications, where start-stop technology can introduce a power down 12 times for every four miles driven. With the average urban driving 25 miles per day, this works out to 250,000 cycles over 10 years.

The purpose of this paper is to provide a better understanding of the relevance of standard strain energy based models for low cycle fatigue of solder joints in predicting the behavior of standard SMT packages subjected to a very high number of power cycles.

/ EXPERIMENTAL PROCEDURE

A RF power supply was subjected to an accelerated life test (ALT). The test conditions for these units are shown below:

- Coolant Temperature:
  - Inlet Air Temperature: 50°C / Inlet Water Temperature: 45°C
- Output Power Cycling:
  - RF ON: 4 min / RF OFF: 1min
- Output Load:
  - Two months at 50 Ohms
  - Four months at 31.3 +J34.3 (complex load)

Three units failed during ALT. Circuit troubleshooting identified the failure sites as 2512 resistors in the gate drive circuit. The last failure initiated after 53,215 Output ON events. Visual examination of the 2515 SMT resistors in the RF Gate Drive circuit revealed problems with solder joint cracking (see Figure 6).
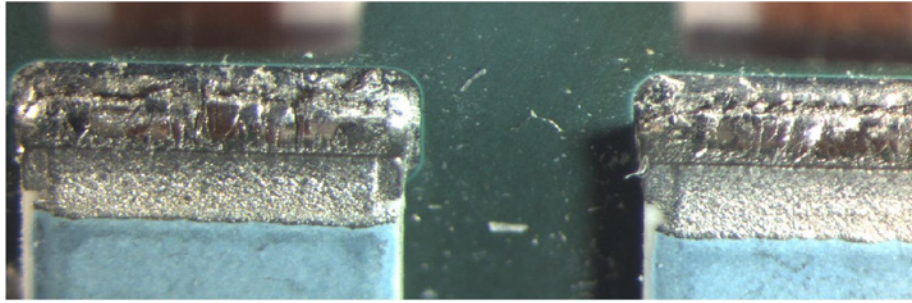
Figure 6. Optical image of failed solder joints at R4 and R5.

To obtain a better understanding of the extent of solder joint cracking, all eight resistors in the RF Gate Drive circuit were cross-sectioned and the cross-sectional views are shown in order from R2 through R9 in Figure 7. Based on the crack propagation path and the phase coarsening observed around the crack path, it was concluded that the solder joint cracking was due to low cycle fatigue. A diagram from a typical solder fatigue is shown in Figure 8 with the cross-section of the failed R5 solder joint.[26] Based on the schematic, the R5 solder joint crack followed a "typical" path starting from the inner end (heel) and propagating until failure occurred.
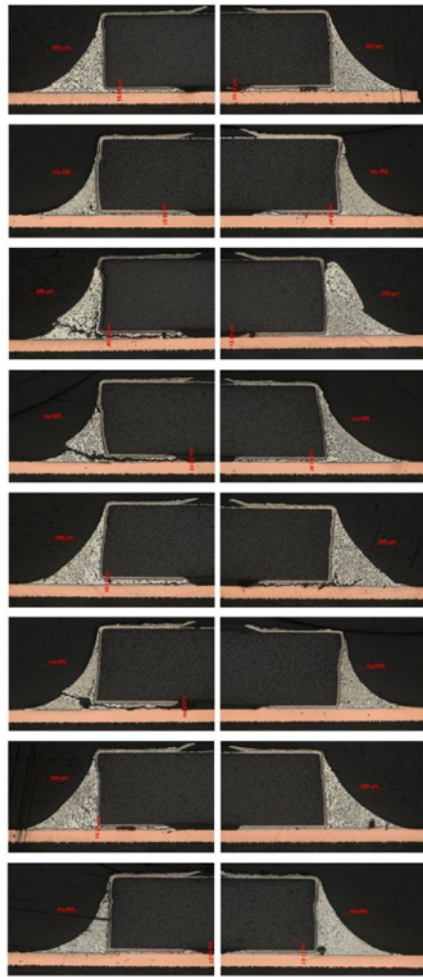

Figure 7. Cross-section views of R2 (top) to R9 (bottom). "Heatsink" end is on the left.
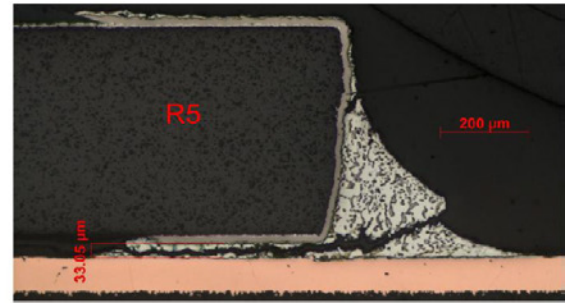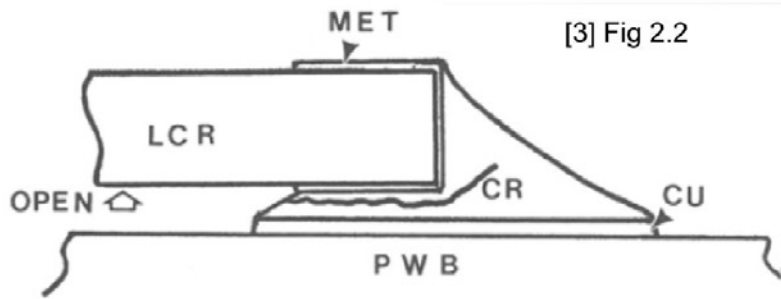
Figure 8. Typical failure diagram from Lui et. al. and a cross-section of the failed R5 solder joint.

To better understand the drivers for solder fatigue under the 2512 resistors, T-type thermocouples were placed on the gate drive resistors (see Figure 9). The temperatures were recorded using a 343970 data logger and a graph of the resistor temperature data for multiple power cycles is shown in Figure 10 and a table of peak temperatures is displayed in Table 1.

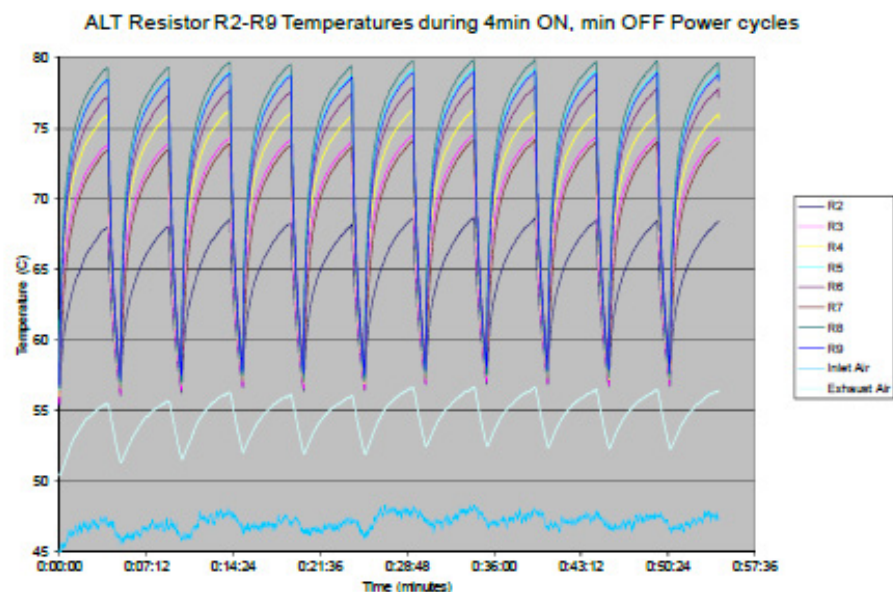Figure 9. Thermocouple placement on gate drive resistors.

Figure 10. Thermocouple data for gate drive resistors.

Table 1. Table of temperatures for gate drive resistors (*temperatures seem low; possible measurement issue).

Resistor	6kW Output Power			0.5kW Output Power		
	Max Temp (°C)	Min Temp (°C)	ΔT (°C)	Max Temp (°C)	Min Temp (°C)	ΔT (°C)
R2*	68.0	55.4	12.6	56.4	47.6	8.8
R3	73.8	55.5	18.3	63.6	48.0	15.5
R4	75.9	56.0	19.9	64.6	48.4	16.2
R5	78.5	56.5	22.1	69.2	48.9	20.3
R6	77.2	56.6	20.6	68.4	49.1	19.3
R7*	73.5	56.9	16.6	63.9	49.3	14.6
R8	79.3	56.6	22.7	71.5	49.4	22.1
R9	78.5	56.8	21.6	70.4	49.7	20.7

/ CORRELATION OF FAILURE BEHAVIOR TO STRAIN ENERGY MODELS

The results from thermal measurements and design and material parameters were inputted into the Blattau model and compared to ALT results. The inputs used for the calculation are shown in Figure 11. The solder joint height (h) of 0.036 mm was determined using a cross-section of a resistor on an unfailed board.

Computes the number of **Cycles to Failure** for a selected package type given solder, PCB and various device properties, as well as a thermal profile. If you select a *Package Name* from the given list, the database values associated with that selection will be automatically entered. You may then override those values as needed. Press the **Compute** button to calculate the results.

Solder Properties

Solder Material:	TIN-LEAD (63SN37PB)
Solder Thickness:	0.036 mm
Cycles To Failure:	50,614
Stress:	2.305e+0
Strain Energy:	3.260e-2

Thermal Profile

Min Temperature:	56.5 C
Min Dwell Time:	1 min
Max Temperature:	78.5 C
Max Dwell Time:	4 min

Board Properties

Board Thickness:	2.8 mm
Board Modulus (E):	15416 MPA
Board CTE:	17.630 ppm/C

Package Properties

Package Name:	2512
Package Units:	mm
Package Length:	6.40
Package Width:	3.20
Package Thickness:	0.6
Package Material:	ALUMINA

Pad Properties

Pad Length:	1.28
Pad Width:	3.2
Pad Material:	COPPER

Figure 11: Inputs for the Blattau model.

It can be seen that the cycles to failure prediction provided by the Blattau model (50,614 cycles) is within 5% of the observed time to failure (53,215 cycles). These results would seem to suggest that plastic strain energy is still a critical driver for solder fatigue under these conditions, even given the short dwell times (4 minutes) and high number of cycles (>50,000).

Additional modeling was performed using a crack propagation proposed by Han and Song[27] specifically for chip resistors, where

$$\frac{da}{dN} = K_3 (\Delta W_{ave})^{K_4}$$

with N = crack propagation life, a = length of crack, K3 = 0.0044 (model constant for SnPb), K4 = 1.3227 (model constant for SnPb), and ΔWave = averaged strain energy density change per thermal cycle. This equation ignores crack initiation (region 1) and assumes that the life is dominated by crack propagation (region 2). Thermal data and finite element analysis (FEA) simulation was used to determine the range of ΔWave based on the Han and Song model. ΔWave was determined to be 0.020MPa for a similar operating profile (5 .67 min ON, 1.33 min OFF) to the ALT application. The ALT failures occurred at 50 °C ambient and an output profile of 4min ON and 1 min OFF, which works out to the equivalent of 0.030 MPa. Using this value of strain energy density and a critical crack length of 1 mm, based on the pad length, gives the following:

$$\frac{da}{dN} = K_3 (\Delta W_{ave})^{K_4} = (0.0044)(0.030)^{1.3227} = 4.26E - 5 \ mm/cycle$$

$$N_f = \frac{a_{crit}}{\frac{da}{dN}} = \frac{1mm}{4.26E - 5 \ mm/cycle} = 23,489 \ cycles$$

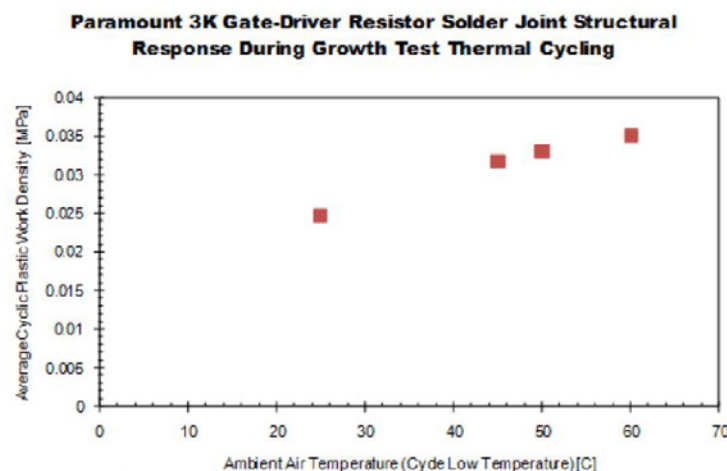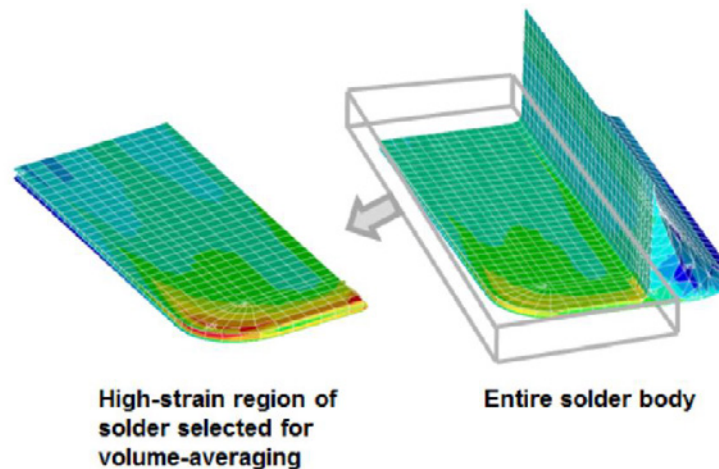High-strain region of solder selected for volume-averaging

Entire solder body

Figure 12. Finite element analysis (FEA) model and estimate of Δwave.

/ ASSESSMENT OF POTENTIAL DESIGN CHANGES

Changes to the circuit design, printed circuit board assembly (PCBA) layout, materials or operating conditions could be used to improve the robustness of the 2512 resistor solder joints under ALT. The Blattau model, due to its higher accuracy, was used to evaluate how particular design changes would influence the expected lifetime. The table below lists the proposed change and the estimated impact to the expected life compared to the baseline.

Description	Comment	CTF Estimate	Solder	Package	Pad L x W (mm)	Ambient (°C)	RF ON/OFF Time	Output Power
Baseline	ALT conditions	50,614	63Sn37Pb	2512	1.28 x 3.2	50	4min ON, 1min OFF	6kW
Change to Pb-free solder	Pb-free solder performs better with low strain energy	279,520	SAC305	2512	1.28 x 3.2	50	4min ON, 1min OFF	6kW
Change Resistor Package to 2010 from 2512	smaller solder joint	71,430	63Sn37Pb	2010	1.28 x 2.5	50	4min ON, 1min OFF	6kW
Lower Ambient Temperature from 50°C to 25°C	more like customer operating temperature	68,727	63Sn37Pb	2512	1.28 x 3.2	25	4min ON, 1min OFF	6kW
Increase Pad Width from 3.2 to 3.5	slightly more cycles for crack to propigate	53,622	63Sn37Pb	2512	1.28 x 3.5	50	4min ON, 1min OFF	6kW
RF Output Power reduced from 6kW to 0.5kW	shows ΔT dependence	66,260	63Sn37Pb	2512	1.28 x 3.2	50	4min ON, 1min OFF	0.5kW

/ CONCLUSIONS

A strain energy-based first-order model is capable of relatively accurate prediction out to 50,000 power cycles with dwell times less than 5 minutes. This would suggest that plastic strain and creep continue to play a critical role in solder joint fatigue, even under conditions that would tend to be extended beyond typical low-cycle fatigue.

For more information, and to request a quote from our Ansys Reliability Engineering Services Team, visit: https://upl.inc/a5b0679

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