DESIGN AND PROCESS GUIDELINES FOR QFNS: MANUFACTURABILITY AND COMPATIBILITY

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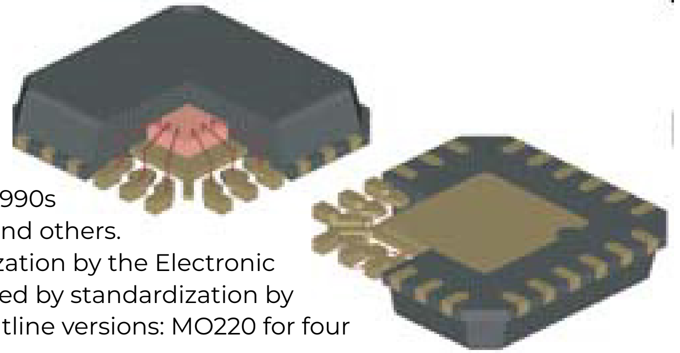
One of the fastest-growing package types in the electronics industry today is the quad-flat no-lead (QFN) package. This package is also known as quad-flat non-leaded (QFN), lead frame chip scale package (LFCSP), MicroLeadFrame (MLF), MLP, LPCC, QLP, and HVQFN. It consists of an overmolded lead frame with bond pads exposed on the bottom and arranged along the periphery of the package.



The basic concept of the QFN was developed in the early to mid-1990s by a number of companies, including Motorola, Toshiba, Amkor, and others. QFN's emergence into electronics was facilitated by its standardization by the Electronic Industries Association of Japan (EIAJ) in mid-1999. This was followed by standardization by JEDEC Solid State Technology Association, which released two outline versions: MO220 for four sided (most common) and MO229 for two-sided.

Since then, the QFN has overtaken the component industry due to its ability to change a perimeter leaded device to an array leaded device at very low costs. It is no coincidence that its nickname is "poor man's ball grid array", as it is expected to dominate lead counts between 8 to 68. Can anyone say "gullwing obsolescence"?

QFNs are currently available from as small as 1x2 mm (3 leads) to 14x14 mm (120 leads). All of these packages are currently single row around the periphery. Dual rows may increase input/output (I/O) count to above 150. Other variations available include singulated vs. sawed and with or without heat sinking.

/ DRIVERS FOR QFN

The introduction of the QFN has tapped into a need to limit the footprint of lower I/O devices, which has been stymied for costs reasons. Primarily, standard ball grid array (BGA) materials and processes are just too expensive. The overall design of the QFN reduces cost up and down the supply chain because component manufacturers are able to package more integrated circuits (ICs) per frame and original equipment manufacturers (OEMs) are able to reduce the overall board size.

Improved thermal and electrical performance are other drivers for the widespread adoption of QFNs. As seen in the image on the right, a standard QFN has a large heat sink under the package. This thermal path from die to heat sink to board is much shorter, more direct, and much larger than most other package types.

The resulting superior performance can then be seen in the table on the next page, the θJa for the QFN is typically about half of a leaded counterpart (as per JESD-51). This can allow for up to a 2X increase in power dissipation with no increase in junction temperature.

Table 1: Thermal performance of QFN compared to similar leaded packages

Package Type	Body Size (mm)	Leads	Height (mm)	Max Die Size	PCB Area	θ Ja
QFN	7 x 7	48	1.00 max	203 x 203 mils	49 mm^2	27
TQFP	7 x 7	48	1.20 max	190 x 190 mils	81 mm^2	55
QFN	5 x 7	38	1.00 max	124 x 202 mils	35 mm^2	34
TSSOP	4.4 x 9.7	38	1.10 max	108 x 207 mils	62 mm^2	73
QFN	5 x 5	16	1.00 max	124 x 124 mils	25 mm^2	37
QSOP	3.9 x 4.9	16	1.75 max	86 x 120 mils	31 mm^2	112

QFNs are also selected for their lower impedance. At higher operating speeds, inductance of the gold wire and long lead-frame traces found in leaded components can start to affect signal integrity and performance. The inductance of a QFN is typically half its leaded counterpart because it eliminates gullwing leads and shortens wire lengths.

Table 2: Inductance values for corner and center I/O of QFN compared to a similar leaded package

	Inductance (nH)	
Package	QFN 7 mm, 48 Lead	TQFP 7 mm, 48 Lead
Die size	4.5 x 4.5 mm	4.25 x 4.25 mm
Center lead	0.067	0.871
Center wire	0.867	0.837
Center total (lead + wire)	**0.934**	**1.708**
Corner lead	0.085	1.010
Corner wire	1.081	0.964
Corner total (lead + wire)	**1.166**	**1.974**

/ PROBLEMS WITH QFN

While the advantages of QFNs are clearly defined, Ansys considers QFN as a "next-generation" technology for non-consumer electronic OEMs due to concerns with:

- Manufacturability
- Compatibility with other OEM processes
- Reliability

Acceptance of this package, especially in long-life, severe environment, high-reliability applications, is currently limited as a result. The next few sections are designed to review the specific concerns in relation to design and process designs by contract manufacturers (CMs) and OEMs and provide possible mitigations or solutions to allow the reliable introduction of QFN packaged components.

Problems: Manufacturability
One of the primary concerns is the ability to repeatedly be able to place and reflow QFNs with a minimum defect rate. While QFNs have been introduced into low-mix, high-volume products with some degree of success, high-mix, low volume operations can experience potential issues. Problems with manufacturability can be divided into stencil design and board design.

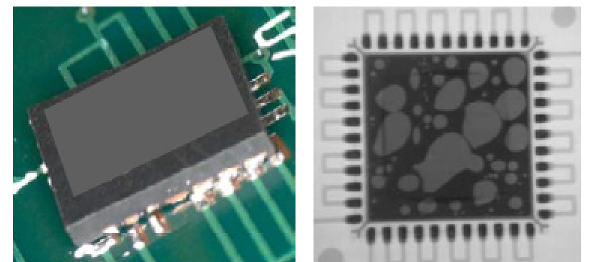


Figure 1: Images of QFN lifting and voiding under the QFN

In regards to stencil design, the stencil thickness and aperture design can be crucial for manufacturability. An excessive amount of paste can induce float, lifting the QFN off the board. Excessive voiding can also be induced through inappropriate stencil design. The appropriate approach is to follow manufacturer's guidelines as much as possible, with a goal of approximately 2-3 mils of solder thickness.

Stencil design for the thermal pad is especially critical for avoidance of the issues listed above. As a general rule of thumb, the ratio of aperture pad should be approximately 0.8:1, with multiple smaller apertures.

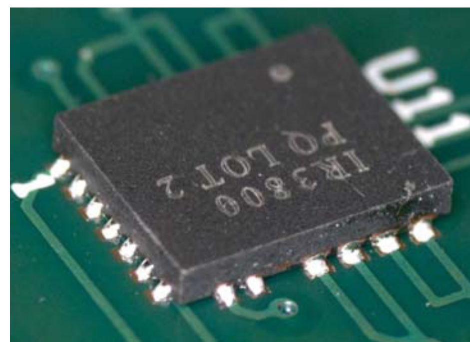


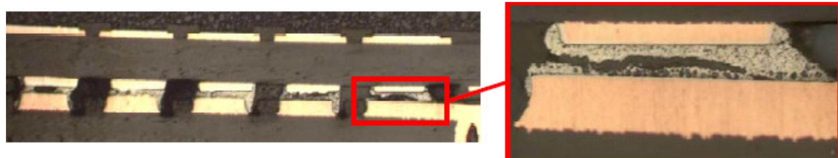
Figure 2: Extension of solder joints due to bond pad design

Board design also plays an important role in regards to manufacturing. To help improve visibility of the solder joint and increase the likelihood of defects captured by visual inspection, board designers should consider extending the bond pad approximately 0.2 to 0.3mm beyond the package footprint. It is important to note that the solder may not always adhere to the cut edge of the QFN leadframe and this behavior should not necessarily be considered as a defect.

Problems: Compatibility

QFNs are also potentially less robustness than other components when exposed to some of the extended ranges of some nominal CM and OEM practices. Of special concern is that the lack of a lead makes QFN solder joints much more susceptible to dimensional changes, either at the part or at the board.

In one case study, a military supplier experienced solder separation under QFNs. After extensive failure analysis and investigation, the QFN supplier admitted that the package was more susceptible to moisture absorption than initially expected. This resulted in transient swelling during reflow soldering, which induced a vertical lift, induced a vertical lift and caused solder separation (see below).



Most interesting about this case study is that the components did not experience popcorning. Acoustic microscopy of the components did not identify any cracking or delamination, but the degree of the dimensional change from moisture absorption was enough to induce defective solder joints.

Another dimensional change of concern is board flexure. Most CMs and OEMs are unfortunately unaware how much flexure their circuit cards experience after reflow. Activities such as in-circuit testing (ICT), functional testing, daughter card insertion, board attachment, and rack insertion can place extremely high stresses on the components attached to the printed circuit board (PCB). Area array devices are especially known to have board flexure limitations because of their limited compliance due to the absence of long, flexible copper leads. The transition to lead-free has made this weakness so inherent, that a number of CMs and OEMs now place maximum microstrain limits during assembly. For some BGAs, this maximum value can be as low as 500 µe.

QFN likely has an even lower level of compliance than BGAs. However, given this risk, there is a surprising lack of studies and quantifiable information on the behavior of QFNs when subjected to excessive flexure. While current QFNs are relatively small (the largest is 14x14 mm, while BGAs can easily be 25x25 mm and larger), this risk will likely initiate unless CMs and OEMs take a conservative approach to design and post-reflow process steps.

For more information, and to request a quote from our Ansys Reliability Engineering Services Team, visit: https://upl.inc/a5b0679

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