TECHNICAL PAPER

Ansys

DESIGN GUIDELINES FOR CERAMIC CAPACITORS ATTACHED WITH SAC SOLDER

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Failure avoidance in ceramic chip capacitors has been accomplished through the development of design guidelines based on physics of failure principles. The transition to Pb-free solder, specifically SnAgCu, has resulted in both a change in processes and materials. This has required a review of current guidelines and modifications where appropriate. Failure mechanisms for ceramic capacitors are presented and the drivers for failure occurrence, mechanical, thermal, chemical, and electrical, are tabulated. The influence of Pb-free solder on each driver is then analyzed, with the subsequent output changes in current design guidelines with justification when appropriate.

/ INTRODUCTION

Avoiding failures in ceramic chip capacitors, also known as multilayer ceramic capacitors (MLCCs), is strongly driven by the ability of the designer, both electrical and mechanical, to follow guidelines based on an understanding on how surface mount ceramic capacitors fail. The transition to Pb-free has required a change in materials and processes, potentially requiring a change or modification in these guidelines. To understand how and when these guidelines must be modified, a diligent listing of potential failure mechanism must be provided. That listing is displayed below:

- Visible Intrinsic Defects
  - Firing cracks
  - Knit lines/delamination
  - Voiding
- Thermal
  - Thermal shock
- Mechanical
  - Placement/handling cracking
  - Flex cracking
- Chemical
  - Dendritic growth
- Electrical
  - Resonance
  - Dielectric breakdown

/ INTRINSIC DEFECTS

Intrinsic defects are anomalies introduced by the component manufacturer that limit the expected lifetime of the ceramic capacitor. In MLCCs, there three basic types of visible internal defects in MLC capacitors that impair reliability: knit lines/delamination, voiding, and firing cracks. Knit lines/delamination, displayed in Figure 2 are cracks that run parallel to the electrodes and are caused by issues with the pressing or sintering processes, which include insufficient binding strength, trapping of air or foreign material, and internal sublimation of burnout material. Voids are large pockets of air between electrodes and are caused by contamination, both organic and inorganic, in the ceramic powder or a non-optimized burnout process. An example is displayed in Figure 3. Firing cracks often originate at an electrode edge, propagate perpendicular to the electrodes, and typically initiate during cooling after densification (see Figure 4).

Since these defects are introduced before the Pb-free soldering process and component manufacturers transitioned to Pb-free plating several years ago, the preponderance and severity of these defects is not expected to change.

/ THERMAL SHOCK

Thermal shock cracks occur due to the inability of the ceramic capacitor to temporarily relieve stresses during transient conditions. The most common signature of thermal shock is a 45-degree microcrack emanating from the termination of the end cap (see Figure 5). While the initiation of a thermal shock crack will not induce failure, if the capacitor is exposed to varying levels of voltage or temperature, the crack will eventually grow, cutting off the electrodes from the termination and inducing an electrical open (see Figure 6). The susceptibility of MLCCs to thermal shock is dependent upon the MLCC architecture, the dielectric material, the solder pad geometry, and the parameters of the soldering process. For example, MLCCs with plated terminations wet about a 100x faster compared to MLCCs with Pd/Ag or Ag terminations. This results in situations where Ni-plated parts can experience 100% failure compared to standard thick film terminations of Ag and Pd/Ag would have no failures when subjected to the thermal shock testing using a wave solder reflow technique[4]. In another study, 1206 X7R MLCCs made from ceramic A with a fracture toughness (KIc) value of 1.3 MPa·m½ and from ceramic B with a (KIc) value of 0.9 MPa.m½ were compared using wave solder reflow[5]. The results show the susceptibility to thermal shock changes, ranging from no failures in the chips with the higher KIc to about a 75% failure rate in those with the lower KIc. This shows that ceramic materials with higher KIc are desirable.

For reflow, no design changes are necessarily required. All existing sizes and designs of MLCCs are reflowable with Pb-free solder, and board bond pad dimensions do not need to be altered. One Pb-free manufacturing concern is the tendency for contract assemblers and industry organizations to promote reflow profiles with higher ramp rates to ensure sufficient throughput (see Figure 7). To prevent thermal shock, ceramic capacitor manufacturers typically provide the following recommended ramp rates:

- Room temperature to preheat (max. 2-3 °C/second)
- Preheat to maximum temperature (max. 4-5 °C/second)
- Cooling (max. 2-3 °C/second)

However, as seen in Figure 7, some part manufacturers and assemblers have higher cooling rates, upwards of 5 to 6 °C/second, to increase the throughput lost from the longer times for preheat and ramp to maximum temperature. In addition, the assembly should be less than 60 °C before being subjected to any cleaning processes such as an aqueous wash.

Design changes should be considered for the more severe reflow processes of wave soldering and hand soldering. Thermal shock is typically prevented during wave soldering by limiting the case size to a maximum of 1210. Due to the more severe conditions of Pb-free wave soldering, designers should consider reducing this maximum case size to 1206 or 0805. Previous experimentation has also shown that thicker capacitors and wider bond pads increase the likelihood of cracking. Therefore, designers should pay attention to these parameters and consider placing limitations, such as no ceramic capacitors thicker than 1.25 mm, or modifying existing specifications, such as reducing bond pad dimensions to below manufacturer's recommendations. As with solder reflow, the parameters of the wave solder should also be maintained. Preheat temperatures should be increased to maintain the same change in temperature upon contact with the solder wave.

Designs that intentionally require hand soldering of MLCCs should be eliminated with the transition to Pb-free, and any rework should be performed with a hot air knife instead of a solder iron as the increase in tip temperature from 300 °C to 350 °C greatly increases the chance of thermal shock during touch-up.

Of special importance is understanding when MLCC failures are not due to thermal shock. Transient thermal analyses performed by Scott[1] and Panchwagh[2] found that the maximum tensile stress during thermal shock events occurs on the boardside of the capacitor, near the termination of the end cap. These model results were validated through the cross-sectioning and inspection of ceramic capacitors believed to have been exposed to thermal shock conditions. Maxwell[3] has also stated that thermal shock cracks occur at or near the ceramic/termination interface (as seen in Figure 5).

There have been some discussions in the literature about the shifting of the crack location away from the termination/ceramic interface. Dematos[4] found that when microdelaminations are present along the electrode/dielectric interface, the location of maximum stress shifts away from the termination to the defect sites. This modeling result was correlated during thermal shock testing, where they found that occurrence of thermal shock failure was strongly correlated with defect population. Those capacitors with fewer and less significant defects were less likely to experience thermal shock cracking.

A similar finding was reported by Anderson5. Capacitors were subjected to best-case and worst-case wave solder profiles, with cooling rates of 0.5C/sec and 15C/sec respectively. No correlation was observed between failure rate and cooling rates. Acoustic examination of all failed capacitors identified internal delamination parallel to the electrodes as the dominant crack morphology (shown in Figure 9).

/ PLACEMENT/HANDLING CRACKING

Placement and handling cracks typically occur during component placement. Since the parameters of this activity are not expected to change with the introduction of Pb-free solder, no changes in design guidelines are necessary.

/ FLEX CRACKING

Flex cracking in ceramic capacitors occurs when there is excessive flexure of the printed circuit board. An example of a flex crack is displayed in Figure 10. Once the flex crack initiates, it tends to propagate at a 45-degree angle from the edge of the termination to the dielectric/termination interface. The creation of a crack path between adjacent electrodes creates the opportunity for internal dendritic growth, shown in Figure 11, resulting in increased leakage current and eventually an electrical short.

Flexure of the printed wiring board can occur throughout the product lifecycle, including depaneling, connector insertion, screw or standoff attachment, in-circuit testing and customer use. Flex cracking of ceramic capacitors is a major driver for field returns due to the ubiquitous nature of ceramic capacitors on today's low voltage designs and high density designs that place ceramic capacitors near potential flex points.

Transitioning to Pb-free was initially a major concern for flex cracking due to the higher modulus and higher yield strength of the SnAgCu compared to SnPb. This stiffer material would theoretically provide a greater transfer of stress for a given displacement (see Figure 12). Initial calculations suggested that the potential failure rate from flex cracking could increase by three orders of magnitude. However, subsequent testing did not prove this to be the case. Experimental studies by Ansys and Kemet demonstrated that ceramic capacitors assembled with Pb-free solders consistently showed similar or improved robustness to flex cracking compared to capacitors assembled with SnPb solder (displayed in Figure 13).

Further investigations identified two potential rationales for the deviation from prediction. First, the reduced wetting of SnAgCu solder creates a greater standoff, imparting additional compliance to the interconnect. Second, the greater stiffness of the SnAgCu solder joint allows the ceramic capacitor to retain a much higher compressive stress after reflow. Any stress arising from board flexure has to effectively overcome this residual stress to induce flex cracking.

While the transition has to Pb-free has not resulted in any changes to existing design rules, mechanical designers should be aware of current design rules to avoid flex cracking. These consist of:

- The board bond pad width should be equal to or less than the capacitor width (eliminate side fillets).
- Maintain a minimum 30 – 60 mil distance from potential flex points (V-score edges, breakoff tabs, separable connectors, attachments).
- If this distance can not be maintained, rotate the capacitor to be perpendicular to the bend radius.
- If the capacitor can not be rotated, consider the use of capacitors with flexible terminations (AVX, Syfer).

/ DENDRITIC GROWTH

Dendritic growth, also known as electrochemical migration, is the migration of metallic filaments under bias through an aqueous solution. It typically requires the presence condensed moisture or contaminants. The presence of condensed moisture can be eliminated through case design or the use of conformal coating and is independent of SnPb or SnAgCu. The presence of contaminants, however, can be very dependent upon the solder material and flux composition being used. Pb-free solders and board platings are much less solderable than SnPb and therefore require fluxes with higher activity to ensure sufficient wettability.

For smaller MLCCs with smaller distances between opposing terminations, care should be taken to avoid using excessive levels of solder paste or flux. If cleaning is desired and a batch process will be used, MLCCs should be placed in areas where they will not be blocked by larger components.

/ RESONANCE

The barium titanate-based dielectric material used in MLCCs is piezoelectric in nature, which results in elastic expansion and contraction with changes in the applied electric field. Typically this displacement is on a microscale and has minimal influence on capacitor behavior. However, at certain resonant frequencies, the capacitor can begin to vibrate along its length. This vibration, if at sufficient magnitude, can induce scattered internal microcracking, resulting in a decrease in capacitance and an increase in leakage current.

The frequencies of concern are typically in the hundreds of kHz to tens of MHz (see Figure 15). The frequency of concern decreases with increasing case size and increasing capacitance. It is currently unknown if exposure to Pb-free reflow will change this behavior, as most characterization of resonance behavior is performed on loose parts.

/ DIELECTRIC BREAKDOWN

The primary mechanism that induces wearout in MLCCs is dielectric breakdown, also known as punch-through. Punchthrough is an iterative process, where areas of current leakage experience self-heating, which deteriorates the insulation resistance of the dielectric, which in turn increases the current leakage. Eventually, a conductive path is formed between adjacent electrodes. To assess the risk of this mechanism, Mogilevsky and Shin developed a time to failure equation where V is voltage, n is a voltage exponent (1.5–7), T is temperature (K), Ea is an activation energy (1.3–1.8) and KB is Boltzmann's constant (8.62 x 10^{-5} eV/K).

$$\frac{t_1}{t_2} = \left(\frac{V_2}{V_1}\right)^n \exp\frac{E_a}{K_B}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

Using previous MLCC designs and highly accelerated testing, this formula predicted that time to 1% failure would not occur for several decades. More recent MLCC designs that incorporate <2.0 µm dielectric thickness have displayed much shorter times to failure. Using data from published literature, time to 1% failure can occur in less than 10 years even under relatively benign use environments (50% derating, 45 °C ambient temperatures).

Most test data on this behavior, as with resonance, has been acquired from loose capacitors that have not been subjected to reflow. Possible changes in this behavior with the application of higher reflow temperatures required for SnAgCu has not been assessed. To ensure sufficient lifetime, designers may wish to consider additional characterization for those capacitors on the board with capacitance/volume (C/V) ratios of approximately 2–10 uF/mm^3.

/ CONCLUSION

As ceramic capacitors are the most common component in today's modern electronics, designers should be made aware of appropriate design rules and potential modifications necessary with the introduction of Pb-free solder to ensure sufficient reliability.

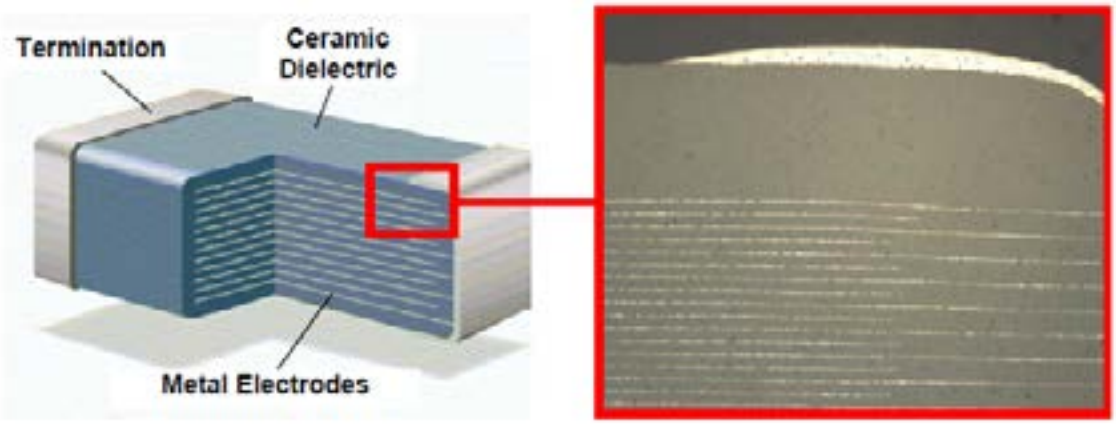

Figure 1. Cross-section of a multilayer ceramic chip capacitor (MLCC)

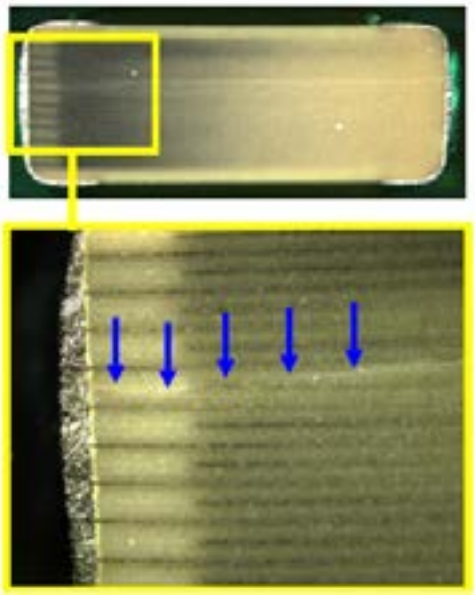

Figure 2. Optical micrograph of a knit line crack in an MLCC

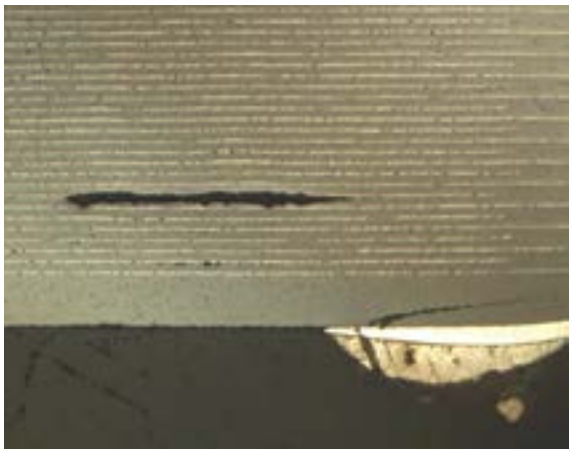

Figure 3. Optical micrograph of voiding in an MLCC

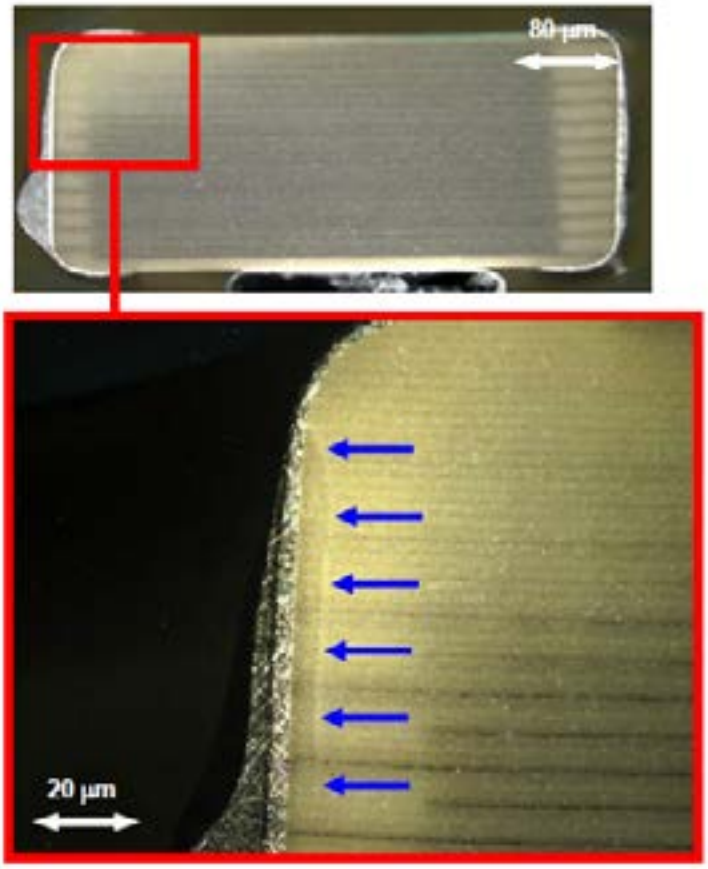

Figure 4. Optical micrograph of a firing crack in an MLCC

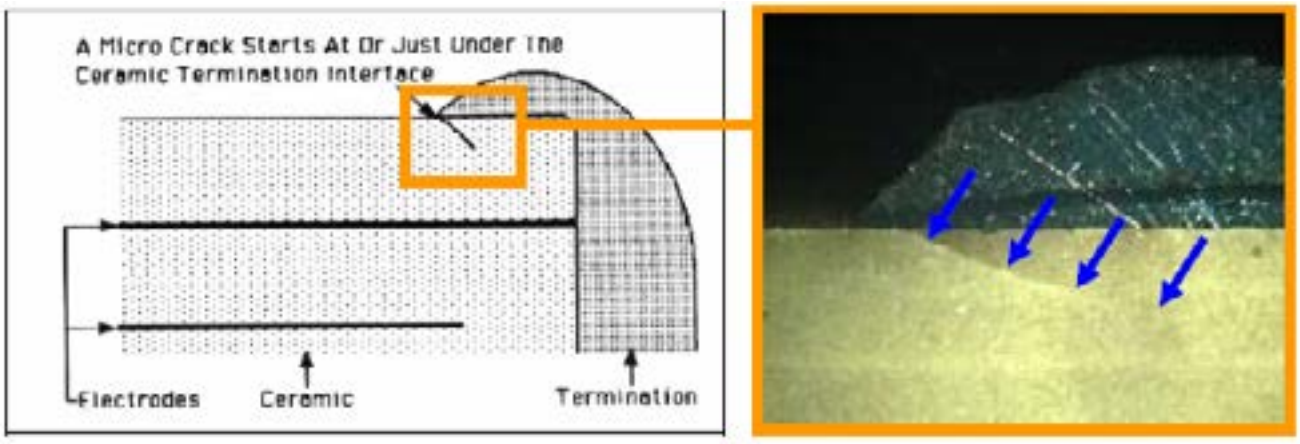

Figure 5. Thermal shock crack in an MLCC (schematic courtesy of J. Maxwell, AVX)

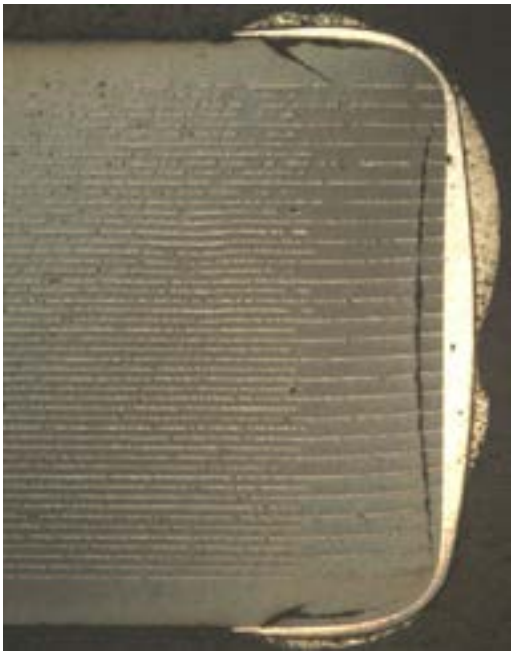

Figure 6. Optical micrograph of a thermal shock crack in an MLCC that has propagated through the metal electrodes

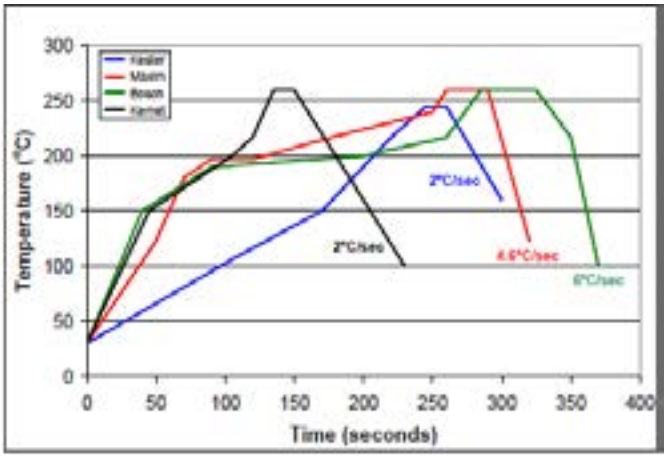

Figure 7. Pb-free reflow profiles from solder supplier, part manufacturer, assembler, and capacitor manufacturer

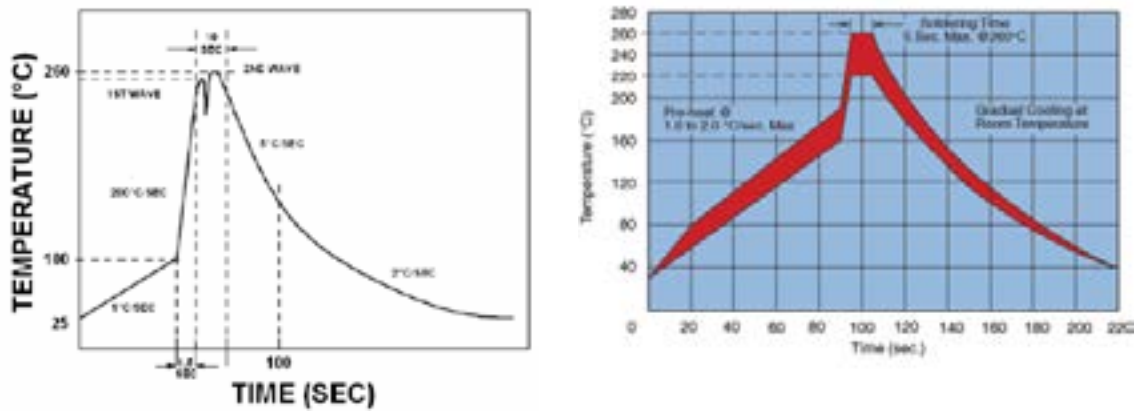

Figure 8. Wave solder profiles for SnPb and SnAgCu solder

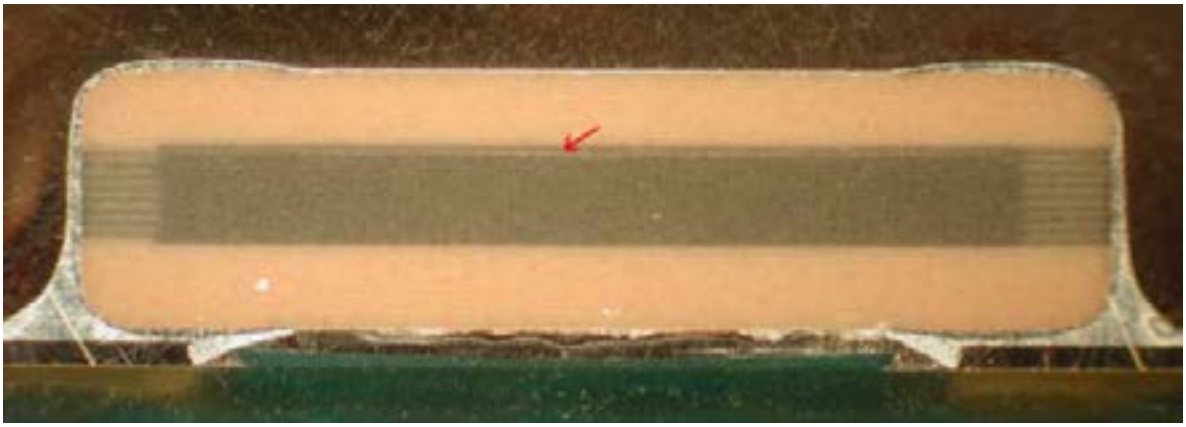

Figure 9. Cracking in an MLCC initially misdiagnosed as a thermal shock crack

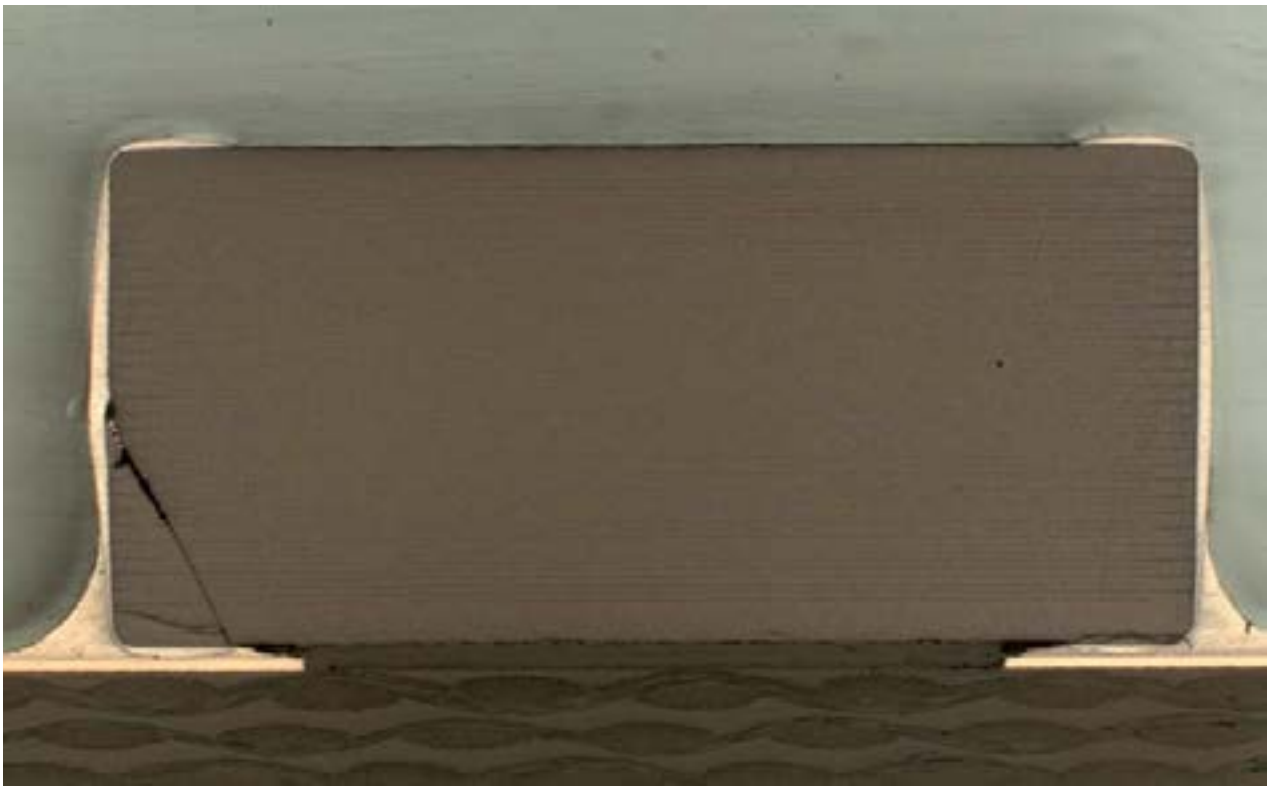

Figure 10. Optical micrograph of flex crack in an MLCC

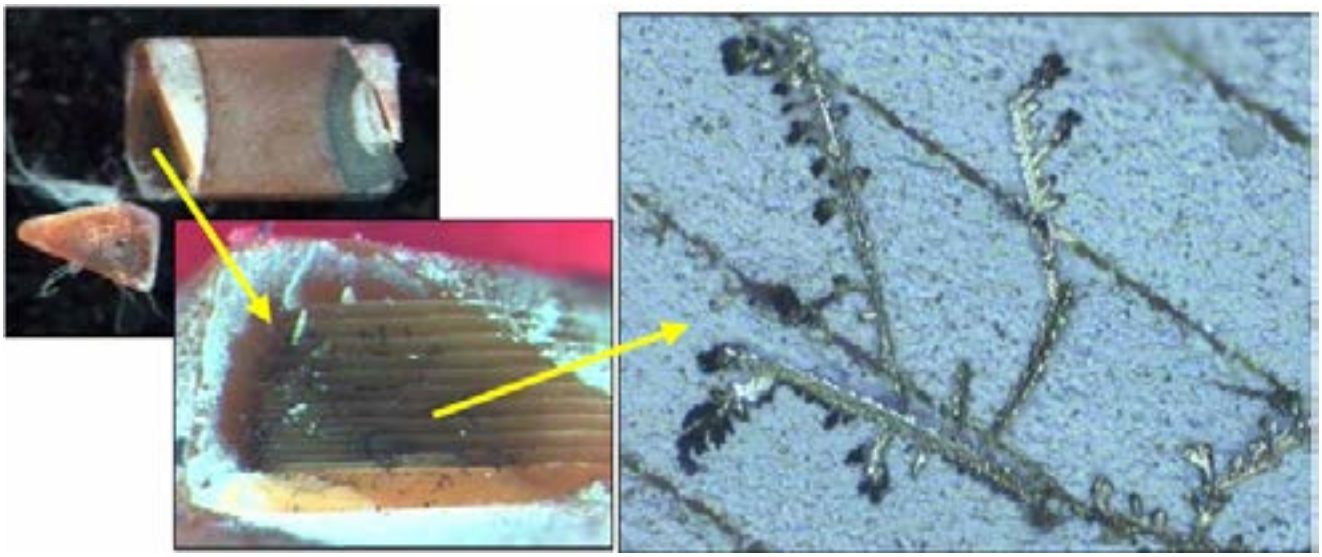

Figure 11. Optical micrograph of dendritic growth in flex crack (courtesy of G. Vogel, Siemens)

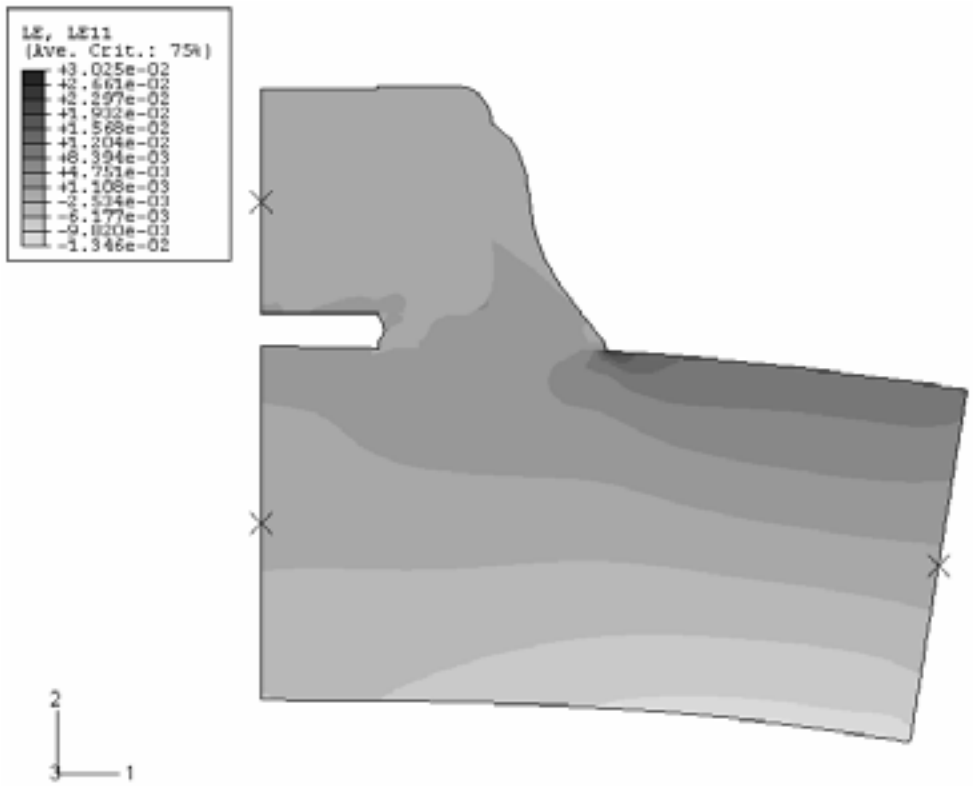

Figure 12. Transfer of stress into the capacitor during board flexure

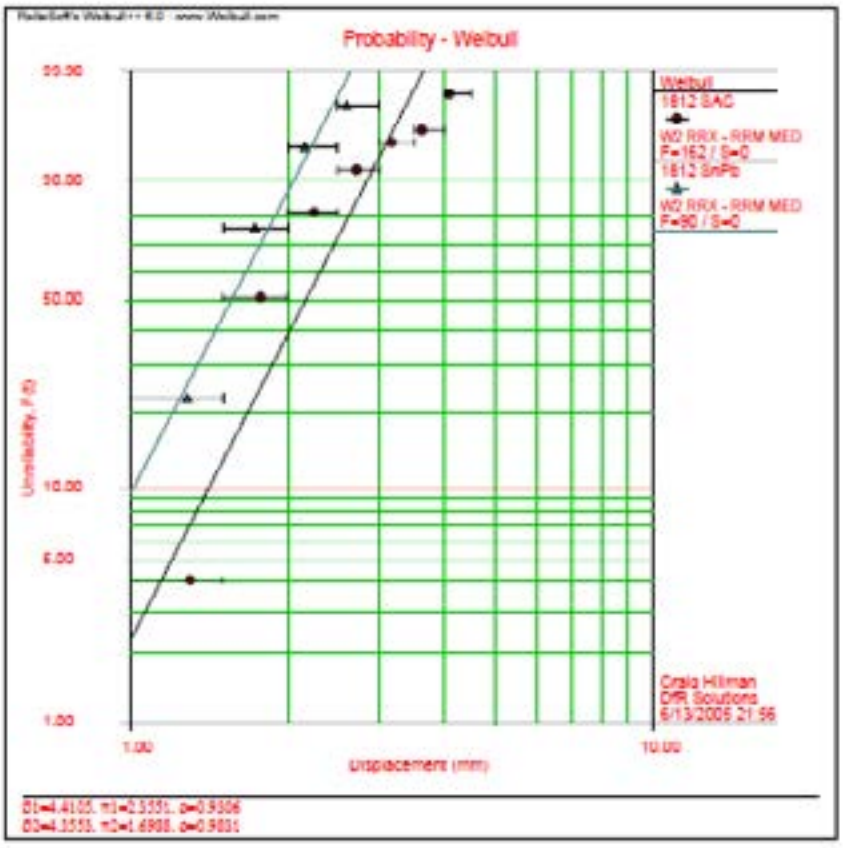

Figure 13: Failure as a function of displacement for 1812 capacitors assembled with SnPb and SnAgCu solder

Figure 14: Optical micrograph of dendritic growth on the surface of an MLCC

Case Size		Resonance Frequency
English	Metric	
3025	7563	250 - 750 kHz
2220	5750	300 - 900 kHz
1812	4532	400 - 1200 kHz
1210	3225	600 - 1200 kHz
1206	3216	600 - 1600 kHz
0805	2012	900 - 1800 kHz
0603	1608	N/A
0402	1005	N/A

Figure 15. Resonance frequencies for various case sizes of MLCCs (courtesy of Nippon Chemi-con, CAT No. E10021)

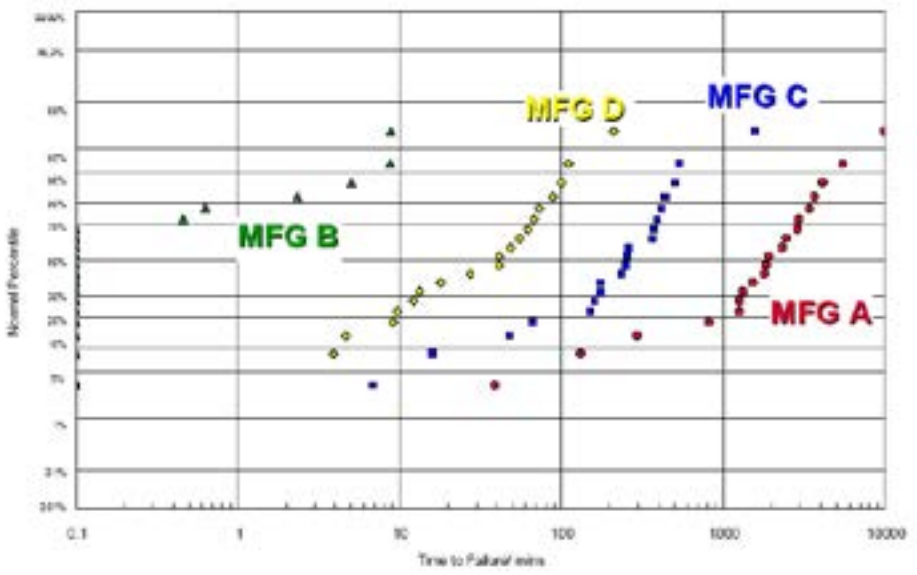

Figure 16. Time to failure behavior of MLCCs with sub-2 micron dielectric (courtesy of Randall, et. al., CARTS 2003)

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