



## THE BENEFITS AND RISKS OF COPPER PILLAR BUMPED FLIP CHIPS

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Traditional solder bumps are being bumped aside by copper pillar technology. Used as a first-level interconnect, copper pillar technology is increasing in popularity as a way to deal with decreasing feature sizes on silicon, mobile device form factors, and other technical challenges of today's flip chip devices. Compared with traditional solder bumps, copper pillar technology provides greater control of the joint diameter and standoff height, enabling the creation of finer pitch joints.

The efficacy of copper pillar has already been demonstrated down to pitches of 80  $\mu\text{m}$  and appears to be a promising approach down to pitches of 40  $\mu\text{m}$ . Along with reduced pitches, copper pillar brings a number of other benefits, including improved electrical performance. However, a balance of design features that impact the die, interconnect, underfill, substrate, and lid must be established to avoid potential reliability issues.

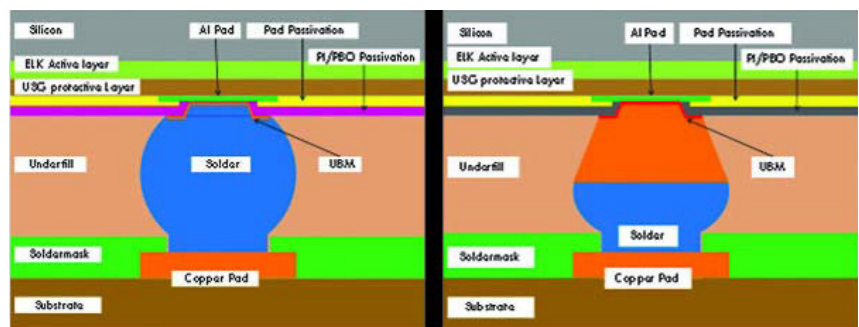


Figure 1. Diagram of conventional solder bump flip chip interconnect design (left); and a copper pillar design (right)

There is much to be learned regarding the reliability of flip chip packages using copper pillar technology. Each manufacturer employs different designs, materials, and process technologies, making it a challenge to improve reliability. Care must be taken when trying to compare copper pillar to solder bump or to generalize results from one copper pillar package to another, because there is such a wide variety of joint designs, materials and manufacturing processes that affect performance.

### The Birth of Copper Pillar

Flip chip package technology using solder bumps to connect the silicon die to the package substrate has been in use for about 30 years. More recently, the use of plated copper pillars as part of the interconnections between the die and substrate was introduced. In traditional solder bump design, the solder forms the entire electrical and mechanical connection between the die and the package. Since the solder melts during the reflow process, the interconnect takes a relatively spherical shape, but the exact dimensions, both diameter and height, are somewhat uncontrolled. Copper pillar technology provides the opportunity to create a cylindrical joint with more control over the diameter and standoff height between the bottom of the die and the top of the package substrate.

Copper pillar technology was patented by IBM in 2001, in the form of a metal post attached by solder to the silicon and substrate pads. By 2005, copper pillar interconnects began to be used in RF power amplifiers. In 2006, Intel used a combination of copper pillars and tin-lead solder joints in its 65nm processors. At the time, Intel documented several benefits of copper pillar technology, including improved electromigration resistance, improved thermal conductivity, simplified underbump metallization (UBM), and higher I/O density.

Many believe that the migration to copper pillar flip chip allowed Intel to avoid the industry-wide problem with low-T<sub>g</sub> underfill, since the company maintained its use of high-T<sub>g</sub> underfill in its copper pillar design (where T<sub>g</sub> is the glass transition temperature). It is also noteworthy that Intel did not mention improved thermal cycle reliability as a benefit of copper pillar over solder bump technology.

Since then, copper pillar technology has grown rapidly. While the market growth of flip chip overall has been moderate and has not gained ground against wirebond technology since 2012, the growth of copper pillar within the flip chip market has been substantial. Copper pillar technology has been widely adopted by outsourced semiconductor assembly and test (OSAT) providers, in addition to major device manufacturers like Intel, TI and others.

The use of copper pillar technology for flip chip represented about 25% of the market in 2010, rose to well over 50% by 2015, and is projected to make up about 75% of the flip chip market by the end of 2018. Copper pillar is likely to become the most dominant type of flip chip interconnect in the coming years.

### Benefits of Copper Pillar

The main driver for the use and growth of copper pillar first-level interconnects is to enable finer pitches. Below about 125µm, solder bump technology reaches its pitch limit. Flip chip assembly using solder requires reflowing the entire interconnect, which produces spherical or barrel-shaped joints.

As pitch is reduced, both standoff height and joint reliability decrease, and the risk of shorts is increased. Copper pillar joints suffer less from these limitations; and are an absolute necessity to enable the latest silicon process nodes of 28nm and below.

Copper pillar joints at pitches from 125 down to 40µm are in use today or have been demonstrated in prototypes or laboratory studies. Copper pillar technology also allows for smaller devices, as demanded by mobile device manufacturers, and reduces the number of package substrate layers, which lowers cost.

### The Question of Reliability

While copper pillar technology offers significant benefits, producing reliable joints requires balancing many factors, often with conflicting effects. A balance of design features impacting the die, interconnect, underfill, substrate, and lid must be established to avoid six major issues:

- Low-k dielectric cracking during chip attach or underfill.
- Warpage, which can negatively impact package coplanarity and thermal interface material (TIM) bond line thickness.
- Flip chip joint reliability in the field, particularly solder fatigue during thermal cycling.
- Die backside stress during chip attach, which could crack the die.
- Second-level solder joint thermal fatigue reliability.
- Electromigration failure.

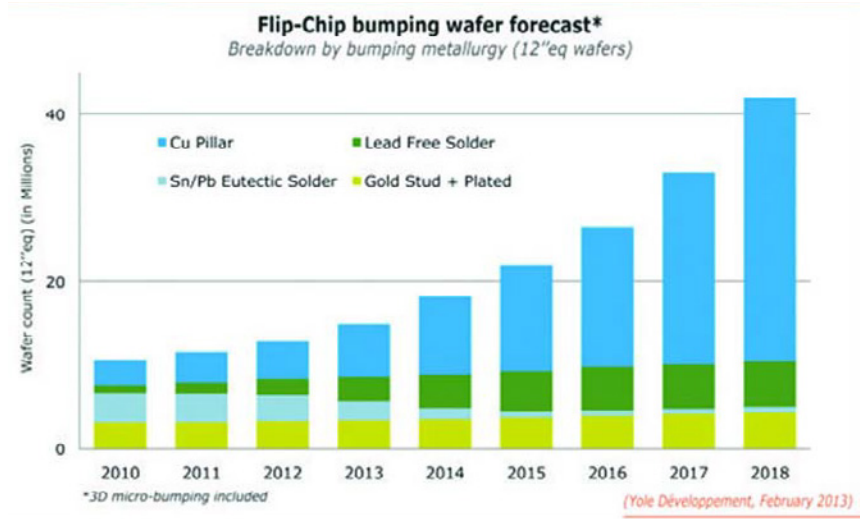


Figure 2. Historical and forecast growth of copper pillar technology within the flip chip market

Given these complexities, one might question whether copper pillar results in packages that are more or less reliable than the traditional solder bump design. It depends; the reason is that there are many variations in flip chip devices and first-level interconnects. There are many different ways to balance the design parameters of the die, interconnect, underfill, substrate, and lid, which in turn impact the severity of these listed issues.

### Design and Process Variations

The reliability of copper pillar flip chip devices depends on the overall design of the flip chip package, the design of the copper pillar joint, and the materials and processes used to create them.

### Flip Chip Package Design Variations

Since its development, the design of flip chip packages has evolved to encompass many forms. Such designs include bare die with underfill, lidded, molded with exposed die and with or without underfill, and overmolded. In addition, stacked chip and stacked package designs are increasingly used today, especially in mobile applications, along with through-silicon via (TSV) designs.

Either copper pillar or conventional solder bump may be used for each of these package types. The differences in materials and physical design can lead to wide variations in mechanical stress and strains within the joints, die and package substrate, and to the current crowding and thermal loads that drive electromigration.

### Copper Pillar Design Variations

In addition to the impacts of package materials and design variations, the copper pillar joints themselves show broad design variability across the industry. The structures vary in pillar dimensions (height and diameter), pillar shape (square, oval or round), pillar wall (tapered or straight), the ratio of pillar height to solder thickness, the ratio of pillar diameter to UBM diameter, the ratio of pillar diameter to bond pad diameter, and the presence/absence of a compliance layer (polyimide).

These variations in joint structure have an impact on the mechanical, thermal and electromigration stresses within the joint and the package. These differences in package and copper pillar joint design complicate any attempt to make reliability comparisons of solder bump to copper pillar, or even copper pillar devices to each other.

### Manufacturing Process Variations

As with package and joint design, the package assembly process varies across the industry. The most common processes are standard reflow (solder paste), modified reflow (flux dip), and thermocompression bonding. For the reflow processes, alignment of the silicon and package substrate is particularly critical. Other steps in the process must also be optimized for acceptable yields and reliability.

Even simple steps, such as the cleaning of the wafer pad surfaces, must be optimized to ensure proper bonding of the copper pillars to the pads, to avoid non-uniform pillar shear strength that could impact reliability.

Thermo-compression bonding is quickly becoming the dominant copper pillar package assembly process, particularly at pitches below 60  $\mu\text{m}$ . This process only takes between two and three seconds to complete, similar to wirebonding. From a reliability perspective, the concern with this process is that the non-conductive paste (NCP) becomes the underfill.

The mechanical properties of NCP are different than those of standard underfill materials, having lower elastic modulus and glass transition temperatures,  $T_g$ . Underfill properties tend to dominate the long-term reliability performance of the joints during thermal cycling, so the thermo-compression bonding process should be examined carefully.

While promising to enable finer pitches than traditional solder bump designs, copper pillar technology raises many issues that are difficult to solve. Reliability is a main concern, with varying challenges in the areas of materials, design and manufacturing processes. Despite these complexities, copper pillar is expected to soon become the most popular form of interconnect technology in today's flip chip devices.

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