SEMICONDUCTORS

Ansys RedHawk-SC

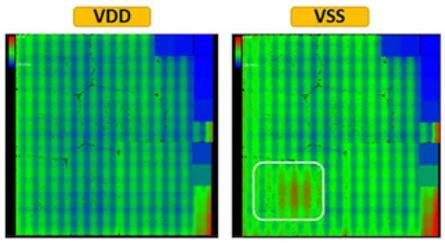
The Industry Gold-Standard for Power Integrity and Reliability Signoff

Ansys RedHawk-SC™ is the industry's trusted gold-standard voltage drop and reliability multiphysics signoff solution for digital designs, certified for all advanced foundry nodes. It provides a comprehensive set of analytics to identify power integrity and reliability weaknesses, along with the tools needed to enable quick fixes of issues for first-time silicon success. Advanced capabilities include SigmaDVD for high local switching-noise coverage and reduced order modeling for efficient full-chip analysis to accelerate design convergence. What-if incremental analysis and tight integration with ECO and static timing analysis tools maximize signoff productivity.

Redhawk-SC's cloud-optimized architecture gives it the speed and capacity to handle full-chip analysis for the world's largest designs. RedHawk-SC is built on Ansys SeaScape™, the world's first custom-designed big data architecture for electronic system design and simulation. SeaScape provides per-core scalability, flexible design data access, instantaneous design bring-up, MapReduce-enabled analytics and many other revolutionary capabilities.

Silicon-Proven Signoff Leader

As the industry gold-standard for SoC power integrity and reliability signoff, RedHawk-SC is supported by certifications from advanced foundry nodes down to 2nm. RedHawk-SC minimizes design risk as the industry's leading solution for power noise and reliability signoff, with hundreds of customer designs in production.



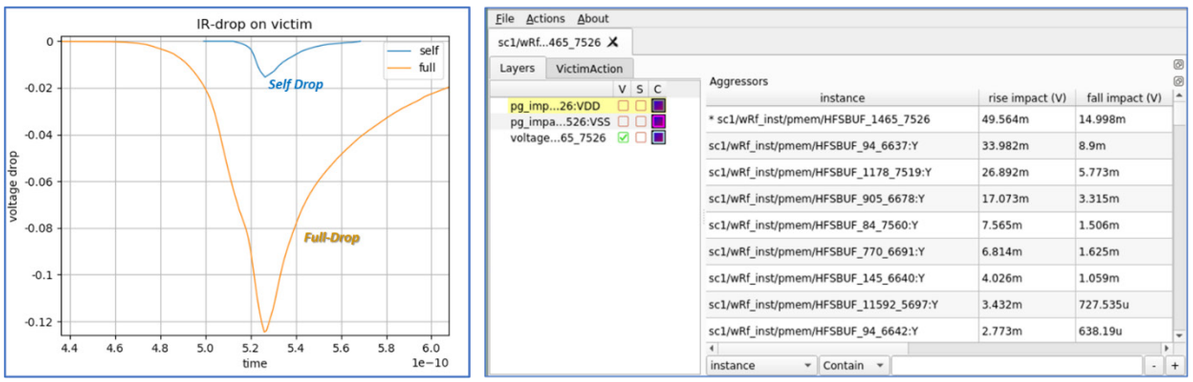
Voltage drop heat maps in RedHawk-SC

Comprehensive Dynamic Analysis

RedHawk-SC provides the most comprehensive dynamic analysis coverage, enabling SoC signoff with confidence using a wide variety of simulation approaches — RTL and gate vectors, smart vectorless analysis for functional and scan modes, and mixed-mode simulation (vectorless and vector-based).

Local Noise Coverage with SigmaDVD

For designs at and below 7nm, local aggressor switching has a dominant impact on voltage drop, amplifying the challenge for coverage across different activity scenarios. RedHawk-SC's SigmaDVD™ is a revolutionary technology that smartly identifies the exact source of power integrity issues across all instances early in the design cycle. SigmaDVD achieves high local-noise coverage without the prohibitive run-time and compute resources associated with a transient DVD approach that would require exhaustive chip level simulations across all possible vectors to achieve the same coverage.



SigmaDVD generates aggressor-victim information to provide high local-noise coverage.

Root Cause Identification and DVD Diagnostics

RedHawk-SC has all the tools needed to quickly debug and root-cause design weakness, voltage drop hotspots, and EM violations using its informative and intuitive graphical user interface and a rich set of analysis tools. In addition, the integrated Explorer allows you to debug input data issues and provides insightful summary data.

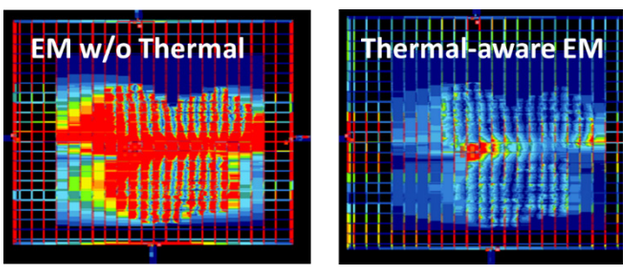
With neighbor-switching becoming the dominant factor for designs at and below 7nm, RedHawk-SC's DVD Diagnostics provides comprehensive aggressor-victim information. Whether using vector or vectorless scenarios, DVD Diagnostics quantifies the impact of aggressors, enabling you to directly fix the root cause of the voltage drop problems with the least effort and impact on your design.

Fast Full-Chip Analysis with Reduced Order Modeling

With designs getting very large, there is a need to efficiently analyze and debug top-level power grid issues early. RedHawk-SC Reduced Order Modeling (ROM) significantly accelerates chip-level analysis for multibillion instance designs, providing the ability to iterate and identify top level power issues early in the design flow. ROM uses significantly less compute resources while maintaining high accuracy of results for top-level construction analysis. It provides an effective way to find grid construction issues at the chip level and to quantify the impact of packaging. It also provides context-dependent impact of chip-level design on blocks.

Electromigration and Reliability Signoff

EM closure at advanced technology nodes requires significantly more complex EM rules to account for shrinking geometries, higher drive currents, and thermal effects. RedHawk-SC provides power and signal electromigration (EM) analysis to address this complexity, in addition to advanced thermal-aware EM and statistical EM budgeting. Redhawk-SC's power and signal EM engines are signoff certified for advanced foundry nodes down to 2nm.



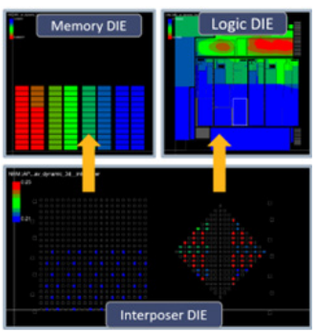
On-chip thermal-aware EM

Multiphysics Optimization

For advanced process nodes, margin-based design methodologies using traditional workflows result in overdesign and guard-banding. The result is not only larger die sizes but also increased design schedules. With a broad set of analytics tools in a single environment, RedHawk-SC enables you to analyze and optimize your design across a spectrum of multiphysics (voltage, thermal, EM) to minimize overdesign.

3D-IC Design Co-simulation

The Ansys RedHawk-SC Electrothermal™ option adds full-system thermal and power integrity co-simulation for chips and 2.5D/3D-IC packages, including package signal integrity and thermal-mechanical stress and warpage, for a broad set of multi-die configurations.



3D-IC concurrent signoff

Accelerated Convergence with What-if Analysis and Voltage drop ECOs

RedHawk-SC's what-if analysis technology significantly improves productivity for ECOs by updating voltage drop results only for affected cells without the need to re-run a full transient simulation. Example ECO changes include cell moves, cell downsizing, and cell deletion.

Combining RedHawk-SC's what-if analysis technology with third-party ECO tools such as Synopsys Tweaker®, the leading timing-driven ECO solution, provides an automated voltage drop ECO flow for the signoff stage that is timing-aware. Also known as IR-ECO, this flow is architected to handle large capacity designs. It leverages Tweaker's

physical-aware placement engine and RedHawk-SC's dynamic IR-drop information to minimize the number of fixes required to your power grid to solve voltage-related timing issues while significantly reducing time-to-convergence.

/ Voltage-aware Timing Analysis

Voltage drop can cause significant impact on delays, especially at advanced geometries. Built on the industry's golden signoff tools for voltage drop, Ansys RedHawk-SC, and timing, Synopsys PrimeTime®, a complete solution is available for voltage-aware timing signoff, also known as the IR-STA flow. RedHawk-SC performs DVD analysis for critical-path aware scenarios, and the voltage waveforms are exported to PrimeTime for timing analysis.

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