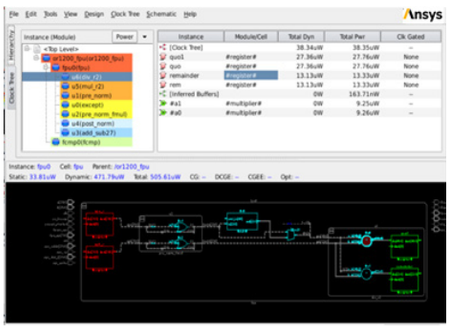
SEMICONDUCTORS

Ansys PowerArtist

Industry-Leading Comprehensive RTL Design-for-Power Platform: Analyze, Debug, Reduce

Ansys PowerArtist™ is the register-transfer level (RTL) design-for-power platform of choice for semiconductor design. From handheld to wall-powered chips ranging from mobile, high-performance processors, networking, automotive and IoT applications, PowerArtist is used to analyze and reduce power early in the RTL development cycle for the highest impact. RTL power from PowerArtist also drives early power grid, thermal, and security analyses.



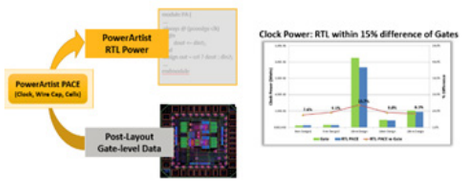
Most Comprehensive Power Analysis and Exploration

Early visibility into power and early detection of power bugs play a vital role in meeting time-to-market and first-silicon success goals. PowerArtist's comprehensive set of features enable activity, average, and peak power analyses with multiple views across design categories, power, and clock domains. Based on an RTL functional abstraction of the design, the best-in-class interactive graphical power debug platform and Tcl-based interface for customized queries enable you to quickly identify and debug power hotspots.

PowerArtist slices and dices power all ways

Timing-Aware, Physically Aware RTL Power Accuracy

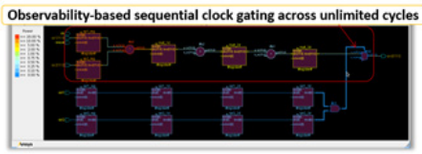
Compared to traditional gate-level methodologies, PowerArtist provides rapid turnaround on multimillion instance designs for fast what-if RTL analysis. PowerArtist's timing-aware cell selection and optimization deliver consistent RTL power accuracy, enabling reliable design decisions. The more advanced the process node, the greater the influence physical design considerations have on power. Pioneering PACE (PowerArtist Calibration and Estimation) technology models design implementation effects including, but not limited to, clock network, wire capacitance, and buffering.



Predictable RTL Power Accuracy

Analysis-Driven Automated Power Reduction

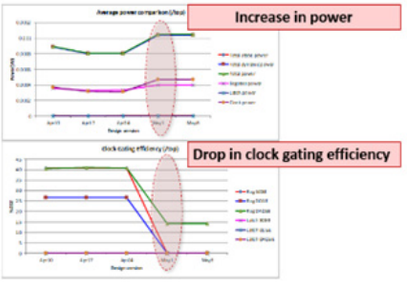
Power efficiency is a critical requirement across applications. PowerArtist identifies all wasted toggles within the design. High-impact techniques identify hierarchical clock and data gating opportunities. Automated combinational and sequential techniques identify new clock enables, redundant memory accesses, and redundant activity in cones of logic with a high-performance architecture not limited to sequential stages. Unique metrics identify glitch-prone logic early at RTL, so designers can target glitch power reduction. Reductions are based on production-proven, physically aware analysis to ensure that identified RTL changes are predictable and minimize design impact.



Predictable RTL Power Accuracy

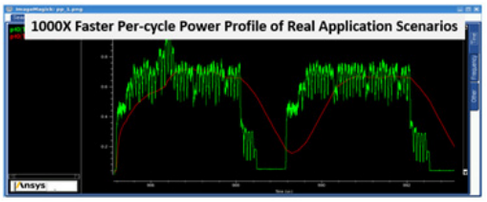
Regressions Based on Power Efficiency Metrics

Regular and rigorous monitoring of power and power efficiency metrics throughout the design development cycle avoids costly, late surprises by isolating power issues when they happen. PowerArtist provides a complete regression framework with well-defined power efficiency metrics, including clock gating and memory accesses, data mining interface, and regression utilities that compare and plot metrics across design versions to prevent power creep. In addition to vector-based detailed metrics, static power efficiency checks can be used during the RTL coding stage when vectors are still not available.



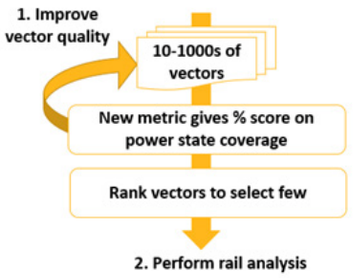
Early Power Profiling of Real Application Scenarios

Traditional power methodologies are based on design activity simulated for a few microseconds, putting the design at risk from power issues that can be exposed by real-world stimuli. PowerArtist provides industry's fastest power profiling, enabling per-cycle analysis of hundreds of milliseconds of activity, such as OS boot-up, within hours — orders of magnitude faster than standard approaches.



Scoring Vectors for Peak Power

Power governs critical design decisions such as those affecting the power grid and the package. The simulation vectors used to estimate power must trigger the worst-case but realistic peak power scenarios to avoid costly design iterations. PowerArtist provides the only solution in the industry that scores vectors for peak power coverage, enabling engineers to assess the quality of the vector and then also target low-coverage hierarchies and leaf instances for testbench improvement to represent the true peak power so you can make reliable design decisions. The scoring metrics can also tremendously aid the identification of the minimum set of cycles that provide the maximum coverage for power grid integrity.

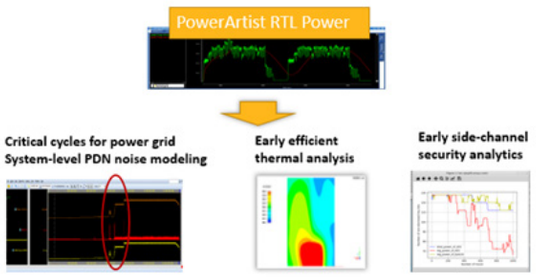


RTL Power-Driven Power Grid Integrity

The power delivery network (PDN) across the chip, package, and system must deliver power across all complex modes of operation. Reduced noise margins at advanced process nodes further challenge the PDN, and it must account for critical scenarios including peak power and di/dt early in the design process. PowerArtist rapidly isolates the power-critical subset of cycles of activity from millions. Moreover, power noise analysis at the system level must account for the low frequency current profile — using only chip-level transient current is not realistic. PowerArtist rapidly generates power profiles across long simulation vectors that are directly consumed by Ansys Chip Model Analyzer™ and Ansys RedHawk-SC Electrothermal™ for a true representation of the full PDN noise.

RTL Power-Driven Thermal Integrity

Thermal issues are a growing concern for high-performance designs affecting performance, reliability, and cost. PowerArtist efficiently consumes emulator-generated activity data for seconds of activity and generates power for transient thermal analysis in RedHawk-SC Electrothermal. This visibility into thermal hotspots, early at RTL, enables timely critical thermal-aware IP and SoC design decisions.



RTL Power-Driven Hardware Security Analysis

Data security and privacy are essential concerns for mission-critical components in many electronic systems. The chip's secure assets can be compromised by exploiting vulnerabilities in the design implementation through side-

channel leakage. PowerArtist's rapid RTL power profiling engines combine with Ansys RedHawk-SC Security™, the breakthrough multiphysics security simulation platform, to provide metrics that can uniquely enable designers to assess the chip's susceptibility to such attacks and to rapidly evaluate design countermeasures, early at the RTL stage.

Emulator Activity Interface

PowerArtist's dynamic activity streaming and critical signal interfaces, along with support of the native activity formats of leading hardware emulators, accelerate the time to power by an order of magnitude. Direct processing of native formats by PowerArtist eliminates unnecessary time and disk usage in conversion to industry-standard activity formats like FSDB.

ANSYS, Inc.
www.ansys.com
ansysinfo@ansys.com
866.267.9724