Modern Memory Interfaces (DDR3) Design with ANSYS Virtual Prototype approach
Agenda

• DDR Design Challenges

• How does simulation solve these design challenges?
  – *Circuit + EM Extraction! (Virtual Prototype)*

• Virtual Prototype
  – Accuracy
  – Speed
  – Capacity
  – Repeatability & Automation

• Summary
DDR X Technology

- DDR3 Design Challenges for Signal Integrity
  - Reduced Voltage Noise Margin

- Standard DDR SDRAMs
  - DDR2 SDRAM
  - DDR3 SDRAM
  - DDR4 SDRAM

- Mobile DDR SDRAMs
  - LPDDR
  - LPDDR2
  - LPDDR3

Output buffer for DDR interface

Without off-chip interconnect.

C_{fixture} (<2~3pF)

\[ \overline{V} \]

1.2V POD (Peudo-open drain)

For AC150

LPDDR

LPDDR2

LPDDR3

Logic Voltage Level & AC/DC Logic Thresholds

Less than 0.52V
Single-ended
without shunt (ODT) termination

<table>
<thead>
<tr>
<th>Standard DDR SDRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2 SDRAM</td>
</tr>
<tr>
<td>DDR3 SDRAM</td>
</tr>
<tr>
<td>DDR4 SDRAM</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mobile DDR SDRAMs</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPDDR</td>
</tr>
<tr>
<td>LPDDR2</td>
</tr>
<tr>
<td>LPDDR3</td>
</tr>
</tbody>
</table>

- Reduced Voltage Noise Margin
• DDR3 Design Challenges for Signal Integrity
  – Reduced Timing Margin

- LPDDR ≤ 400Mbps
- LPDDR2 ≤ 1066Mbps
- DDR2 ≤ 1066Mbps
- LPDDR3 ≤ 1600Mbps
- DDR3 ≤ 2133Mbps
- DDR4 ≤ 4266Mbps
• Design challenges?
  – Validation
    • Prototype
    • Measurement
    • Interpret and implementation (calculation) of Design Spec such as DDR3, LPDDR2 and more…
    • Large amount output data report of results
  – Capacity or Complexity and Time
    • Chip to Chip or Chip to PKG
    • Chip + Package + PCB + Connector/Cable + PCB + Package + Chip
    • Full System
ANSYS Solution

Images and models courtesy of the Xilinx, Micron Technology, TE Connectivity.
## Table of Contents

- Design Summary
- Solution Setup
- Per-Lane
- Per-Edge

### Design Summary

**Description**
- Project: bsys_best_0012_test
- Design: DDR3
- Design ID: 141
- Design Type: Circuit Design
- Location: F:\WORK_2012\09_DDR\Test_Kim\Test
- Date: 9/20/2012 11:03:57 AM
- Product Version: Designer 6.0
- UDD Version: DDR3 Compliance Report, 1.0 (R14)
- User: unassigned

### Solution Setup

**Solution Details**

- Name: DDR3 AC-Timing S-DQ1
- UDO: C:\Program Files\Ansys\Designer 6.0\Windows\sys\:
- Parameters:
  - AC DQ Level: AC150
  - Speed Bin: Auto (from DDR3)
  - DQI delay: 0ps
  - External Report: off

**Per-DQ**

<table>
<thead>
<tr>
<th>DQ</th>
<th>Min [ps]</th>
<th>Max [ps]</th>
<th>Mean [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>DQ0</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>DQ2</td>
<td>615.567</td>
<td>616.405</td>
<td>616.513</td>
</tr>
<tr>
<td>DQ4</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>DQ5</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>DQ6</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>DQ7</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
</tbody>
</table>

**Per-Lane**

**AC Timing (JESD79-3E, Section 13.1)**

<table>
<thead>
<tr>
<th>Metric</th>
<th>Worst Actual</th>
<th>Worst</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tdv(base)</td>
<td>153.504</td>
<td>78.304</td>
</tr>
<tr>
<td>Tdv(base)</td>
<td>212.071</td>
<td>112.071</td>
</tr>
<tr>
<td>Tdv(dest)</td>
<td>64.5042</td>
<td>10.497</td>
</tr>
<tr>
<td>Tdv(dest)</td>
<td>153.071</td>
<td>35.673</td>
</tr>
</tbody>
</table>

**Tvb(base) - Timing Metrics**

<table>
<thead>
<tr>
<th>DQ</th>
<th>Min [ps]</th>
<th>Max [ps]</th>
<th>Mean [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>1</td>
<td>615.567</td>
<td>616.405</td>
<td>616.513</td>
</tr>
<tr>
<td>2</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>3</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>4</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>5</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>6</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
<tr>
<td>7</td>
<td>153.504</td>
<td>152.133</td>
<td>153.965</td>
</tr>
</tbody>
</table>

## Per-Edge

**Tvb Derating Calculations**

<table>
<thead>
<tr>
<th>DQ0</th>
<th>time [ns]</th>
<th>err(DQ0) [V/mV]</th>
<th>err(DQ) [V/mV]</th>
<th>del_Tvb [ps]</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>2.00481</td>
<td>4.100179</td>
<td>None</td>
<td>None</td>
<td>DQ not tested</td>
</tr>
<tr>
<td>1</td>
<td>3.02186</td>
<td>4.65983</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>2</td>
<td>3.98944</td>
<td>4.758</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>3</td>
<td>4.90449</td>
<td>4.77146</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>4</td>
<td>5.84355</td>
<td>4.67474</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>5</td>
<td>6.70016</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>6</td>
<td>7.68929</td>
<td>4.58410</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>7</td>
<td>8.67540</td>
<td>4.75767</td>
<td>None</td>
<td>2.07657</td>
<td>03</td>
</tr>
<tr>
<td>8</td>
<td>9.59340</td>
<td>4.50844</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>9</td>
<td>10.5305</td>
<td>4.72517</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>10</td>
<td>11.4684</td>
<td>4.76814</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>11</td>
<td>12.4089</td>
<td>4.71986</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>12</td>
<td>13.3474</td>
<td>4.60549</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>13</td>
<td>14.2864</td>
<td>4.70259</td>
<td>None</td>
<td>2.21921</td>
<td>03</td>
</tr>
<tr>
<td>14</td>
<td>15.2257</td>
<td>4.68664</td>
<td>None</td>
<td>2.67105</td>
<td>03</td>
</tr>
<tr>
<td>15</td>
<td>16.1605</td>
<td>4.7294</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>16</td>
<td>17.0933</td>
<td>4.63123</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>17</td>
<td>18.0364</td>
<td>4.68233</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>18</td>
<td>18.9762</td>
<td>4.69132</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>19</td>
<td>19.9107</td>
<td>4.70578</td>
<td>None</td>
<td>2.29316</td>
<td>05</td>
</tr>
<tr>
<td>20</td>
<td>20.8489</td>
<td>4.67143</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>21</td>
<td>21.7861</td>
<td>4.69557</td>
<td>None</td>
<td>2.45382</td>
<td>03</td>
</tr>
<tr>
<td>22</td>
<td>22.7242</td>
<td>4.6737</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>23</td>
<td>23.6630</td>
<td>4.73413</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>24</td>
<td>24.6096</td>
<td>4.71855</td>
<td>None</td>
<td>None</td>
<td>DQ not switching</td>
</tr>
<tr>
<td>25</td>
<td>25.5594</td>
<td>4.72779</td>
<td>None</td>
<td>2.55260</td>
<td>01</td>
</tr>
</tbody>
</table>

**Tva(base) - Timing Metrics**

<table>
<thead>
<tr>
<th>DQ</th>
<th>Min [ps]</th>
<th>Max [ps]</th>
<th>Mean [ps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>257.728</td>
<td>601.624</td>
<td>412.427</td>
</tr>
<tr>
<td>1</td>
<td>234.232</td>
<td>122.172</td>
<td>212.122</td>
</tr>
<tr>
<td>2</td>
<td>241.248</td>
<td>667.318</td>
<td>412.390</td>
</tr>
<tr>
<td>3</td>
<td>258.837</td>
<td>637.599</td>
<td>444.067</td>
</tr>
<tr>
<td>4</td>
<td>224.949</td>
<td>637.401</td>
<td>412.277</td>
</tr>
<tr>
<td>5</td>
<td>217.788</td>
<td>640.731</td>
<td>412.839</td>
</tr>
<tr>
<td>6</td>
<td>212.071</td>
<td>650.340</td>
<td>431.930</td>
</tr>
<tr>
<td>7</td>
<td>228.904</td>
<td>649.738</td>
<td>432.244</td>
</tr>
</tbody>
</table>

**Note:** Timing values calculated for extended slewing valid

---

© 2012 ANSYS, Inc. November 14, 2012
Simulation Technology

• Solutions & Benefits
Design Review (1/2)

- Main Board Side
  - No termination resistors for all signals
  - Point-to-Point Interconnect topology between FPGA and SODIMM
  - Controlled skews by serpentine traces
  - Layer Stackup: 16 layers, 2mm Thickness, 8 power planes,
  - Substrate: FR4
  - Board size: 139.7mm x 266.7mm
Design Review (2/2)

- **SODIMM Side**
  - Data Group Signals: Point-to-Point Topology with series termination resistor
  - Clock/Address/Command Signals: Fly-by-Topology

Ex) CAS signal with pull-up end termination

Vtt termination rail
Simulation Technology 1/3

- Hybrid Solution
  - Main PCB, SODIMM PCB, SODIMM Connector

Connector (S-Parameter from Vendor or Simulation)
Simulation Technology 2/3

- Full 3D FEM and Prism
  - Main PCB, DIMM PCB, 204pin Connector (Full 3D EM Model)

HFSS™ Connector + PCB

n-Node Component from HFSS

Sentinel PSI™

Main PCB

DDR3 Socket

DDR3 soDIMM
Simulation Technology 3/3

- HFSS Solver on Demand,
  - HFSS in Designer can handle full 3D interconnect PCB, PKG and Package on PCB Model
Simulation Technology

- Critical Net in HFSS
  - Add full 3D HFSS interconnect Model include ALL(PKG, Connector, PCB)
Post Layout Simulation (1066Mbps)

- Differential Clock Signal

Differential Clock Signal

![Graph showing differential clock signal with peaks at +350mV and -350mV.]

DDR3 SDRAM

Memory

Controller

soDIMM Connector

Odd mode propagation

+350mV

-350mV
Post Layout Simulation (1066Mbps)

- Data group signals
Post Layout Simulation (1066Mbps)

- Data group signals
  - Write Operation / ODT (on-die-termination) Disabled
Post Layout Simulation (1066Mbps)

- Data group signals
  - Write Operation / ODT(on-die-termination) Disabled
- Setup Margin Calculation (before derating)

\[
\begin{align*}
\text{DATA0} + \text{DATA1} + \text{DATA2} + \ldots + \text{DATA7} \\
\text{Vref} = 0.75V \\
\text{AC150} \rightarrow \text{Vref} + 150mV \rightarrow \text{VIH.AC} = 0.9V \\
\text{AC150} \rightarrow \text{Vref} - 150mV \rightarrow \text{VIL.AC} = 0.6V
\end{align*}
\]

Valid Before Time \(T_{vb} = 152\,\text{psec}\)

75psec setup time from receiver (JEDEC) specification

The earliest strobe signal at Vref.diff

77 psec Setup Margin
Post Layout Simulation (1066Mbps)

- Data group signals
  - Write Operation / ODT (on-die-termination) Disabled

- Setup Margin Calculation (with derating value)

The extended derating value ($\alpha$) = 108 ps

Setup Margin = 77ps$^1$ – 108ps = –31 ps

1) setup time (without derating)
• UDS (User Defined Solutions)
Why ANSYS UDS?

- UDS (User Defined Solutions) allows calculations and post-processing of simulated or raw transient simulation data
  - Supported thru IronPython scripting
  - Designer .sdf solutions file
  - H-Spice .tr0 solutions file
  - Useful in Virtual Compliance calculations for different standards

- Key benefits:
  - AC Data Timing Calculations (tDS, tDH, derate ...)
  - Non-Ideal voltage supply is supported
  - Every bit-by-bit falling and rising transition edge is calculated
  - Fully customizable through Python scripts.
    - Templates currently exists for LPDDR, DDR2 and DDR3 standards
Post Layout Simulation (1066Mbps)

- Data group signals
  - Write Operation / ODT(on-die-termination) Disabled
- ANSYS UDS(User Defined Solution) for DDR application

Valid Before Time (Tvb)

Setup Margin without derating value = Tvb (151.86..ps) – setup time (75ps)

Setup Margin through derating value = Setup Margin wo derating (76.86xxps) - Derating value (α, 108ps)

Derating Value is automatically calculated!!! (After comparing tangential slew rates through UDS.)
• Data group signals
  - Write Operation / ODT(on-die-termination) Disabled
• Hold Margin Calculation (before derating)

Post Layout Simulation (1066Mbps)

- **DATA0 + DATA1 + DATA2 + … + DATA7**
- **DC100 → Vref+100mV → \( V_{IH,DC} = 0.85V \)**
- **DC100 → Vref-100mV → \( V_{IL,DC} = 0.65V \)**
- **Valid After Time \( T_{va} = 160\,\text{psec} \)**
- **100psec Hold time from receiver(JEDEC) specification**
- **The latest strobe signal at Vref.diff**

ANSYS DesignerSTM
Post Layout Simulation (1066Mbps)

- Data group signals
  - Write Operation / ODT(on-die-termination) Disabled

- Hold Margin Calculation (with derating value)

  ANSYS DesignerSI™

Valid After time ($T_{va}$) = 160 psec

Hold Margin (without derating value) = $T_{va}(160$psec$) - hold time(100$psec$) = 60$psec$

Hold Time for DC100 & 1066Mbps

Hold Margin through derating value = Hold Margin w/o derating(60$psec$) - Derating value($\alpha$, -74$psec$) = - 14 $psec$
• Data group signals
  - Write Operation / with ODT 120/60/40 Ohm

- Negative Setup Margin!
  - Hold margin with derating value is also positive.

ODT 40Ohm at DDR3 SDRAM
UDD (User Defined Document)
UDD Slides

- **UDD include**
  - Design Summary, Simulation Setup
  - Per-Lain, Per-DQ and Per-Edge Calculation
  - HTML Report support Hyperlink and automatic Post Processing.
Summary

• Modern Memory Interfaces (DDR3) Design with ANSYS Virtual Prototype approach
  
  – Power of EM & Circuit Simulation
    • The combination of ANSYS Solution are very helpful to get insight for your SI problem in all direction
  
  – Easy Validation
    • UDS, UDD

  – Virtual Compliance Test
    • H/W engineers can prevent from logical malfunction through SI simulation and optimized the system performance through what-if simulation.