# Electrical Resistance Modeling of Solid Oxide Fuel Cells

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**Abstract**

Solid Oxide Fuel Cells (SOFCs) offer advantages in efficiency, fuel flexibility and environmental concerns in the production of electrical power. Minimizing the electrical losses in the interconnects of planar SOFCs is of critical importance in preserving the efficiency of the stack. Finite element modeling of the electrical resistance of the interconnect components provides a method of optimizing the stack design. Several ANSYS models were developed to help understand the effects of sheet resistance of the cathode and the contact resistance between various components. An analogous field method is used with steady state thermal conduction models representing the electrical conductivity.

## Introduction

Fuel cells are projected to play an important role in future energy production by providing efficient and environmentally benign electrical energy. A fuel cell is an electrochemical device that converts the chemical energy in the fuel directly into electrical energy without combustion. This direct conversion eliminates the thermodynamic limitations of the Carnot cycle, thus promising the possibility of significantly improved efficiency. The absence of combustion also eliminates the formation of pollutants, including NOx, SOx, hydrocarbons, and particulates.

SOFCs are one of several types of fuel cells currently under development. SOFCs offer the possibility of internal reforming of hydrocarbon fuels and consequently can use diesel, gasoline or natural gas without requiring an external reformer. Designs include tubular and planar configurations. Planar type cells offer higher power density due in part to shorter current paths which lowers the electrical resistance, Planar designs are usually stacked vertically to achieve the required power output. This vertical stacking requires an interconnect between each individual cell which must electrically connect the cells in series while keeping the fuel and oxidant separate. The electrical resistance losses in the interconnect must be minimized in order to maintain the efficiency of an SOFC stack.

### *Theory*

This report describes a method for using ANSYS to model the electrical resistance of the interconnect components by an analogous field representation. Earlier ANSYS manuals describe the use of ANSYS to solve a wide variety of mechanics problems by the analogous field method. It is recognized that the field equations for the representation of a heat conduction problem are identical to those for electrical conduction. Consequently, ANSYS can be used for modeling the electrical conductivity problem by defining a steady state thermal conductivity analysis and substituting the necessary variables. The temperature variable then represents the voltage, the thermal conductivity represents the electric conductivity (1/resistivity), and the heat flux represents the current.

The Poisson equation for a field problem is of the form:

$$\nabla^2(\mathrm{K}\psi) = -q$$

In a heat transfer analysis,

$\mathrm{K}$ = thermal conductivity, $\psi$ = temperature, $q$ = heat flux.

In an electrical conductivity analysis,

$\mathrm{K}$ = electrical conductivity or 1/electrical resistance, $\psi$ = voltage, $q$ = current.

### *SOFC Specifics*

The attention of this modeling effort was focused on the cathode side of the interconnect. The sheet resistance of the cathode ceramic material is much higher than the anode which contains a significant percentage of nickel. Consequently, higher power losses are expected on the cathode side making it more attractive for optimization. The sheet resistance of a typical cathode material was measured and used in the analysis.

The typical current collector in a planar SOFC often consists of a conductive screen or in-plane grid on the electrode. In research settings, conductors (perovskites such as cobaltites or precious metals such as platinum) are used on the cathode to ensure good conductivity. A metallic interconnect structure serves the dual purpose of providing the flow channel for the fuel/oxidant and continuing the current conduction path to the interconnect. Conductive pastes are often used to ensure contact between the interconnect and the in-plane conductive screen or grid. Testing supported by scanning electron microscopy has confirmed the formation of an oxide scale on the metallic interconnect under the correct conditions of materials and operating conditions. This scale has been demonstrated to have high electrical resistance and can significantly decrease the power output from the cell. Any modeling should have provisions to represent this resistance.

## Procedure

Three dimensional models of a unit cell (1 cm x 1 cm) SOFC were constructed using SHELL57 elements. Distinct element types were used to identify the cathode, grid, paste and interconnect. CONTAC173 elements were used with TARGET170 elements to represent electrical contact between the different components. The contact stiffness of the CONTAC173 elements provided a means to account for the effects of the scale resistance. Figure 1 shows the model with the interconnect material removed. The grid coverage and spacing pattern were variables in the optimization. The model shown in Figure 1 represents a 3 x 3 grid providing 56% coverage of the cathode. Additional models were constructed for 19%, 64%, 75%, and 90% coverage. A current of 1 A/cm$^2$ was applied uniformly on the cathode.

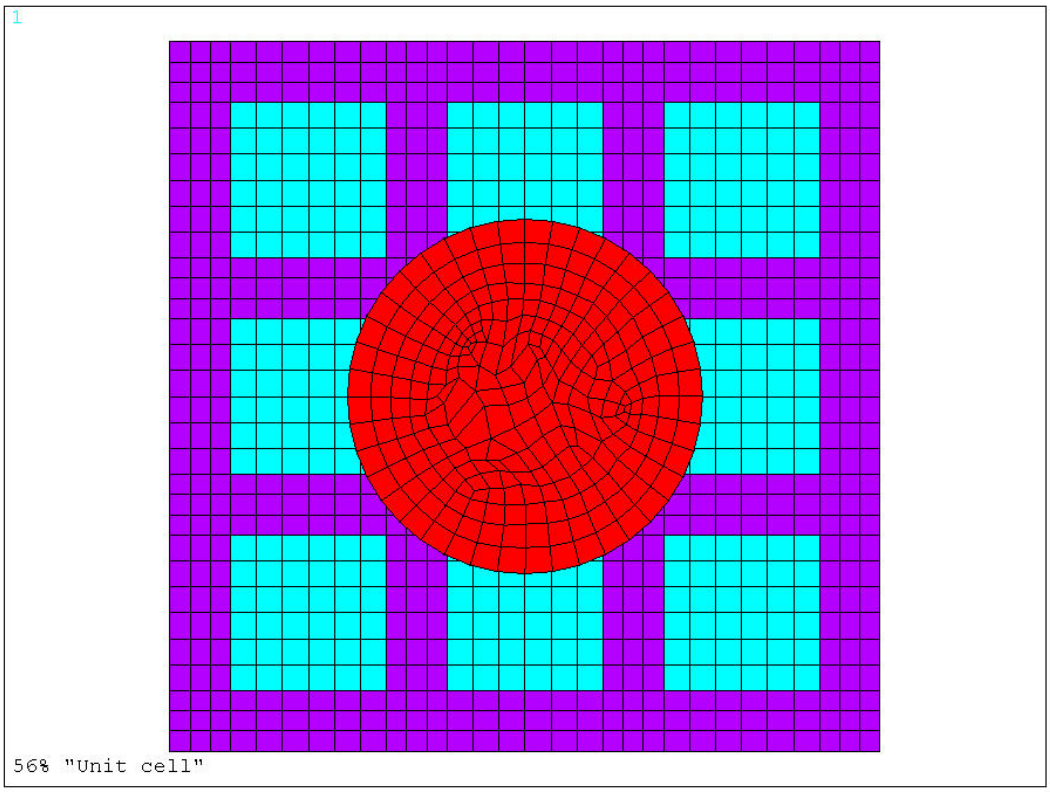


**Figure 1. Model of the cathode, grid and paste (56% coverage)**

## Analysis

Power losses in electrochemical devices are usually defined in terms of voltage drop, also known as polarization or overpotential. Figure 2 shows the overpotential at the cathode with a 3 x 3 grid and 56% coverage. The voltage drop was summed in an ETABLE variable and the average overpotential calculated for each configuration.

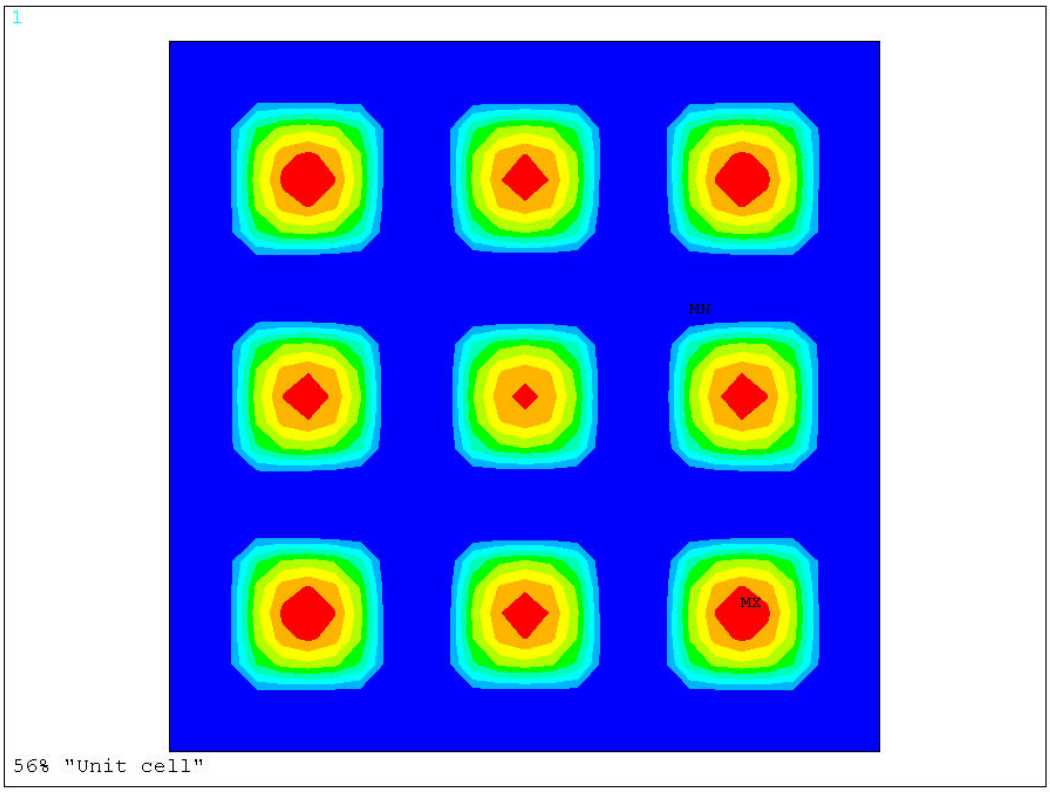


**Figure 2. Cathode voltage overpotential (56% coverage)**

## Analysis Results & Discussion

Figure 3 shows the overpotential as a function of grid coverage. Decreasing the grid coverage has the effect of lengthening the current path through the relatively high resistance cathode and results in increased voltage drop. This is demonstrated more clearly in Figure 4 which shows the overpotential from a 19% coverage 3 x 3 grid as compared to 19% coverage 1 x 1 grid. A model without a grid was also run and the results plotted on this figure. An optimum grid configuration can be defined as one that minimizes the distance from the paste to all points on the cathode.

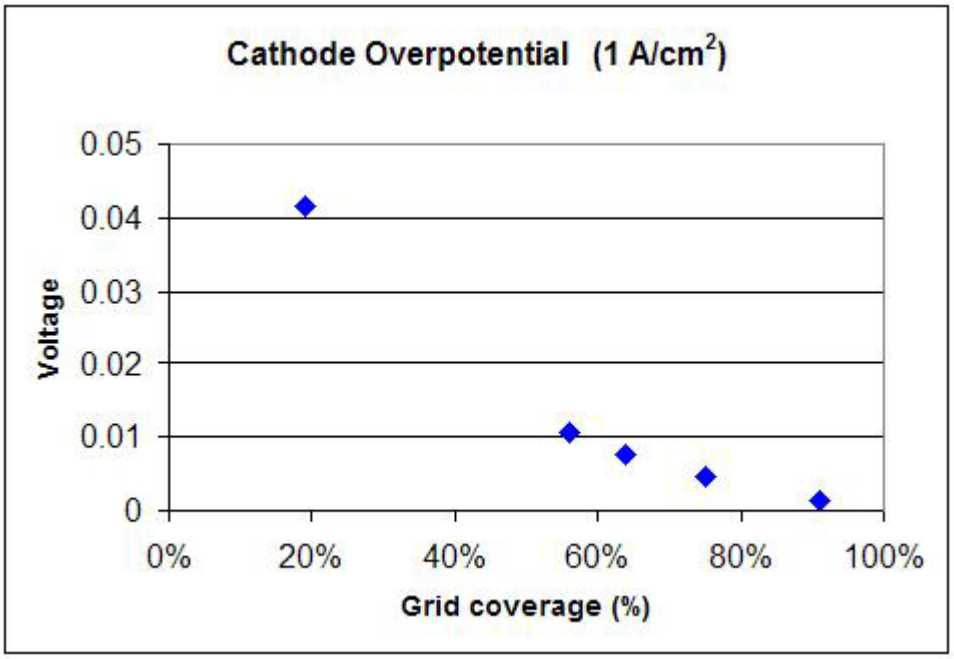


**Figure 3. Comparison of grid coverage**

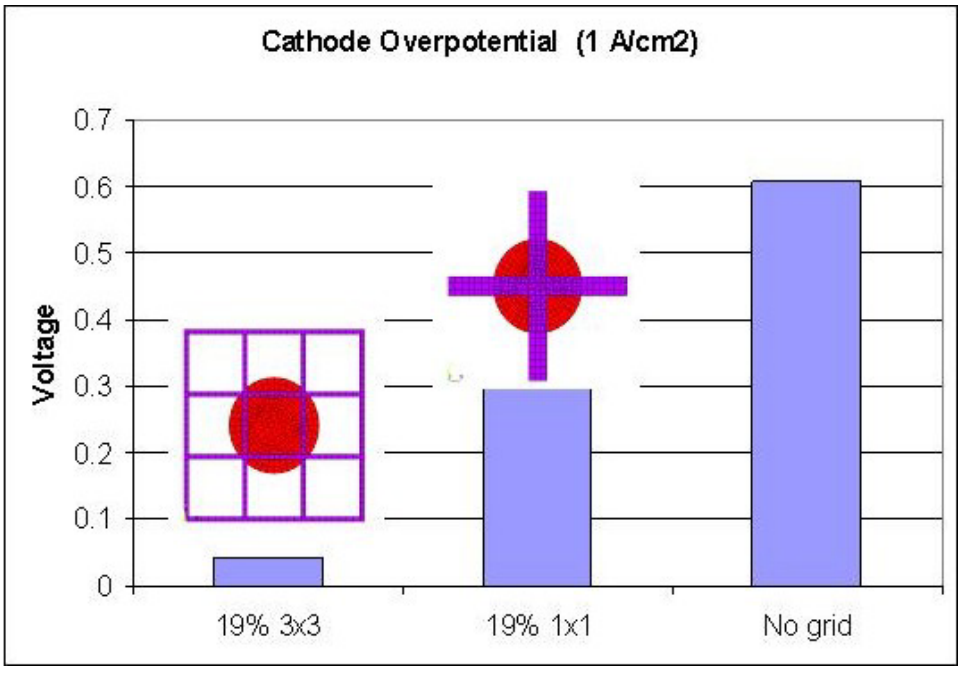


**Figure 4. Comparison of grid pattern**

## Conclusion

An ANSYS thermal analysis can be readily used to analyze electrical conductivity models. Having recognized the similarity in field equations, only a simple substitution of variables is required. This method was used to optimize the interconnect design of an SOFC stack.

### *References*


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2. Bathe, K.J., Finite Element Procedures in Engineering Analysis, Prentice-Hall, Inc., Englewood Cliffs, NJ, 1982.