# REFRESH YOUR MEMORY


**Ooma saved 50 cents on each of hundreds of thousands of devices by using ANSYS tools to design a DDR3 subsystem that does not require a termination voltage regulator.**

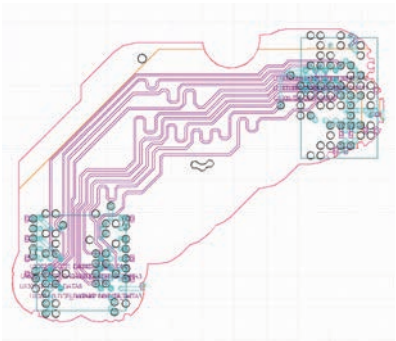
**By Michal Smulski,** Hardware Engineer, Ooma, Palo Alto, U.S.A.

Consumer electronics manufacturing is all about being first to market with a reliable product at a lower cost than the competitors'. These days, nearly every consumer product contains embedded memory to support the logic core that delivers device functionality. Using low-cost standard commodity memory requires that devices comply with double data rate (DDR) standards issued by the Joint Electronic Devices Engineering Council (JEDEC). The DDR interface consists of signals for control, address, clock strobe and data that are transmitted between the memory controller and DDR dynamic random access memory (DRAM).

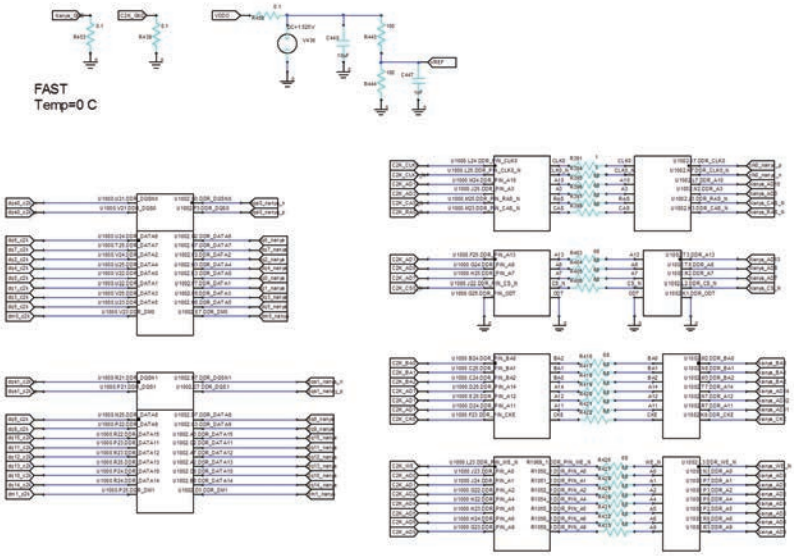
Ooma, which is working to re-invent home telephone service, supports a DDR3 standard on its latest-generation devices that delivers higher performance, but with this performance comes tighter signal integrity requirements for the memory controller. The company's engineers met this challenge by using ANSYS electronic simulation software and tools to simulate performance of the DDR interface in the early stages of the design process, then iterate to an economical solution that avoids the need for a termination voltage regulator.

**Consumer electronics manufacturing is all about being first to market at a lower cost than competitors.**

Ooma offers consumer and business products that provide free and low-cost U.S. and Canadian telephone calling as well as advanced cloud-based telephony services to its global base of customers. One of the greatest challenges on a recent new product was designing the DDR3 subsystem at the lowest possible cost while getting the design right the first time. The DDR3 subsystem resides on a system-on-chip (SoC) with an ARM microprocessor core. The DDR runs at 533 MHz, and data is clocked on both rising and falling edges for a total bandwidth of 1,066 Mbit per second. The initial concept design was created using Cadence® OrCAD®



▲ Extracted subset of Allegro layout including memory chip, controller and traces, and assigned ports used to model data byte 0 in Designer-SI.




▲ Schematic page for simulation (top). All extracted trace models are placed here and connected to package and buffer models. Each box is an HFSS model of DDR3 traces.

Capture and Allegro® layout tools. Ooma engineers connected the components, generated the net list, routed traces and generated the Gerber files used to fabricate the printed circuit board (PCB).

On slower-running buses, the engineering team sometimes performs signal integrity calculations by hand. But the speed of this bus generated concerns, particularly about timing — the ability of the design to produce a valid signal at the DRAM within the time frame allowed by the specification. Signal integrity was another concern, specifically that parasitics created by the PCB traces might distort the signal. The normal starting point to meet these specifications is to use design rules that specify the geometry of the traces, such as their maximum length and spacing. But with this signal speed, rules of thumb are not sufficient to ensure that the design will work. Allegro offers a signal integrity tool, but Ooma engineers felt it was insufficient for this problem because it lacks 3-D simulation capabilities. Engineers instead used ANSYS electronics tools, which provide a complete timing and signal integrity solution that includes a full 3-D model. Another advantage of ANSYS tools is that the engineering team has the ability to simulate antennas, which are used in an increasing number of Ooma products.

**Engineers needed to design the DDR3 subsystem for a new product at the lowest possible cost while getting the design right the first time.**

The SoC and memory vendors provided buffer IBIS models and parasitic package models of their products. The interconnect model was directly exported from Allegro to ANSYS DesignerSI via ANSYS ALinks, which streamlines the transfer of design databases from popular third-party EDA tools into ANSYS simulation products. Models for the data, address and control buses were extracted with ANSYS HFSS, an electromagnetic field solver package. The full DDR3 design was created in Designer-SI and simulated with ANSYS Nexxim, a circuit engine for high-speed channel design. The 3-D HFSS model of the interconnects between the controller and memory accounts for capacitance, inductance, coupling, resistance to ground, resistance to power and inductance to power. The design consisted of 40 data, address and controls signals. Ooma engineers generated 3-D models of these signals by grouping them based on trace location and function to limit memory requirements to reasonable levels.

**DDR VIRTUAL COMPLIANCE USING ANSYS DESIGNERSI**
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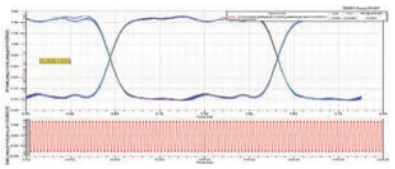
Engineers analyzed the simulation results with the ANSYS DDR Compliance Toolkit to provide a quick verdict on the ability of the design to meet the DDR3 specification. The simulation provided an eye diagram that combined the shape of every possible waveform that could be generated by the design; the diagram is used to visualize and diagnose performance. With this design flow, engineers quickly updated the design — for example, by inputting a different design rule and rerouting the traces — and determined whether or not the new design would meet the DDR3 specification.

The high-speed switching signals used in DDR3 memory generate reflections that cause the signals to overshoot and undershoot the voltage specification, making it challenging to meet design targets. The data signals are terminated in the memory controller, which eliminates reflections on these wires. But there is no internal termination on the control and address signals. Simulation of an early version of the design showed that these reflections would make it impossible to meet the DDR3 specifications. A relatively simple solution is to add a termination

**This entire project was completed in a few weeks without involving expensive signal integrity consultants.**

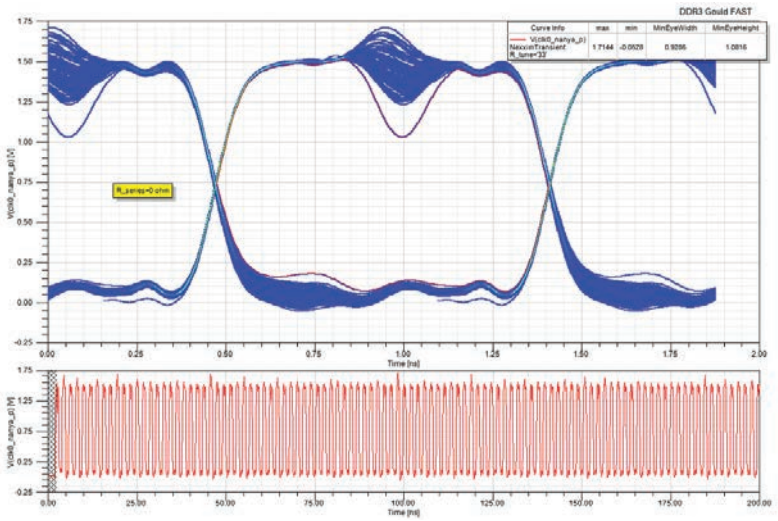


▲ Differential clock eye diagram without series termination

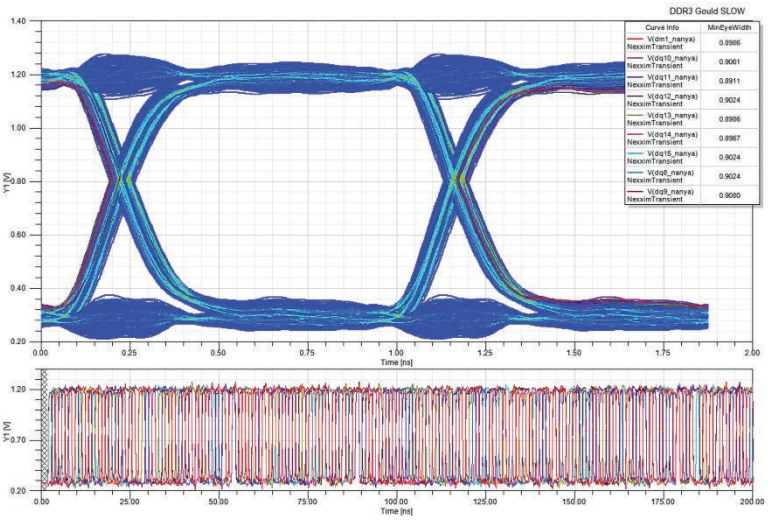
voltage regulator to terminate these wires, at a cost of about $.50. But this is a significant cost when multiplied by hundreds of thousands of units.

To avoid this expense, Ooma engineers tried terminating the control and address lines with an inexpensive series resistor between the controller and memory. The resistor is not as good at controlling reflections as a termination voltage regulator, so signal integrity simulation at various corner cases becomes much more critical. The higher the value of the resistor, the better the job the resistor does in damping the reflections. However, larger resistors tend to round off the leading and trailing edges of the signal, which makes it tougher to meet the timing specification.

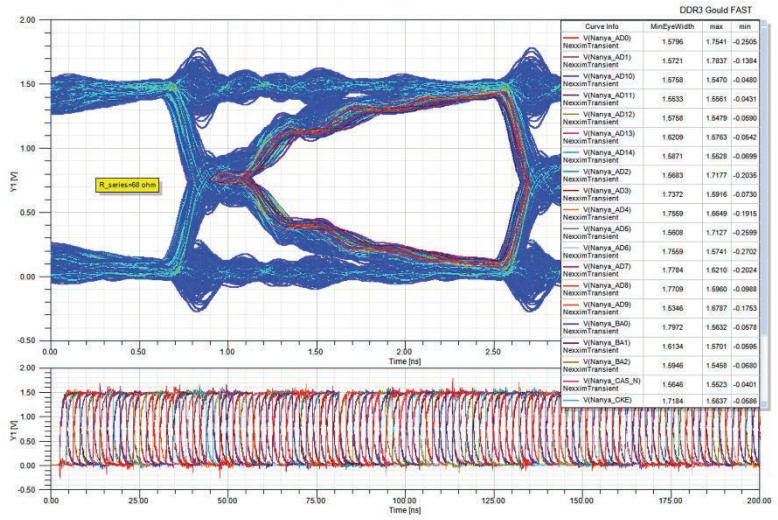
In this case, Ooma engineers swept the value of the resistor from 0 ohms to 100 ohms, while using the simulation to determine the impact on timing and signal integrity. They also made further adjustments in the PCB traces. In the end, the iterated design meets signal integrity and timing requirements without a termination voltage regulator. This entire project was completed in a few weeks by a single design hardware engineer without involving expensive signal integrity consultants. The validated design was then manufactured, tested and FCC certified; it is currently in mass production.




▲ Singled-ended clock eye diagram




▲ Eye diagram of data signal with 60 ohm internal termination




▲ Single-ended DDR3 address and control signals with 68 ohm resistor termination. With this value, the design passed AC overshoot and undershoot specifications.