SMART, CONNECTED PRODUCTS require more functionality in smaller multivariant packages. As the global power budget is reduced and the operating frequencies required to deliver rich features increase, engineers are confronting the issue of power supply noise. The chips, packages and printed circuit board all contribute to power supply noise, so the complete system must be optimized to limit noise across the voltage and ground terminals of the transistors for error-free performance. STMicroelectronics engineers used ANSYS tools to identify and correct a power integrity problem in the complex design of a DDR system that might have otherwise delayed the product launch.

By Déborah Cogoni, Laurent Schwarz and David Auchère, Signal & Power Integrity Engineers, STMicroelectronics, Grenoble, France
In developing a reference board for a new DDR system, STMicroelectronics engineers needed to achieve signal and power integrity within a tight schedule. Optimizing this design required modeling everything, including the on-chip DDR physical device (PHY), the protocol to connect a PHY, memory chips, packages, printed circuit board (PCB), decoupling capacitors and so on. STMicroelectronics engineers used ANSYS Electronics Desktop and SIwave to simulate the complete system design in the frequency and time domains. They found and fixed a problem that, if not detected early, might have required another design spin. The integrated simulation methodology provided by the ANSYS signal and power integrity toolset reduced the time required to validate multiple configurations from two or three weeks in the past to just one week.

SIMULATING THE COMPLETE SYSTEM

The DDR system can be used with a single PHY for multiple memory configurations, including single or multiple DDR2 or DDR3 chips. Engineers needed to test signal and power integrity compliance with each possible memory configuration in the reference board design. Customers often design their own boards based on the reference board, and STMicroelectronics supports customers using spinoffs of the reference board design.

STMicroelectronics engineers began the simulation process by importing the electrical model of the integrated on-chip DDR (PHY model and patterns), package and board created by their designers, and various memory chip models provided by manufacturers into SIwave. Engineers then solved the imported structures and performed multiple simulations to compute resonances, trace characteristics, discontinuity reflections, intertrace coupling and the like. Engineers extracted S parameters, an IBIS interconnect model and a full-wave SPICE model. These were imported into ANSYS Nexxim, SIwave’s circuit simulator, for time- and frequency-domain analysis.
The team used Nexxim to generate time-domain eye diagrams and to check the data timing and voltage for overshoot and jitter. The port excitations were set by drivers in IBIS format, using a pseudo random bit sequence (PRBS) to reproduce real use cases. Eye diagrams are used to indicate the allowable window for distinguishing bits from each other at the receiver end. The required height of the window is given by the noise margin of the receivers. The eye diagram initially showed differential skew between the byte lanes. Depending on the PRBS setting, DQ (data) signals overlapped one another.

**DIAGNOSING THE PROBLEM**

To diagnose the problem, STMicroelectronics engineers used ANSYS SIwave to analyze the complete system power delivery network, including dies, packages, PCB and discrete coupling capacitors. The edge rate issues seen in the eye diagrams were traced to power plane noise. The charge needs to be supplied at a broad range of frequencies that depend on the edge rate. The decoupling capacitors must support this frequency range; for the reference board, they were originally specified based on the data sheets, which is a one-size-fits-all approach.

Engineers used SIwave to calculate power-plane impedance as a function of frequency with and without capacitors. The results showed that with no decoupling capacitors there is a high impedance peak of approximately 100 ohms. With the decoupling capacitors specified based on the data sheet, maximum impedance was reduced to 7 ohms, 1/14 of the original value, but still large enough to cause the problems seen in the original eye diagrams.

“This method has reduced DDR system validation time by 50 to 66 percent, and has become the standard workflow at STMicroelectronics.”
ITERATING TO AN OPTIMIZED DESIGN

STMicroelectronics engineers then ran SIwave’s automated decoupling capacitor analysis to properly dampen resonances within the power delivery network while taking decoupling capacitor parasitic inductance and mounting location into account. SIwave uses a genetic algorithm that enables users to constrain impedance peaks, as well as the number, type and cost of capacitors, as part of the cost function. The optimization algorithm iterated to a new design with specific decoupling capacitors that again allowed reducing the new impedance peak of power delivery network up to 1.1 ohms on high-bandwidth frequency.

The simulation showed that the drain supply voltage (VDD) swing was well within the specifications of the integrated circuits used in the reference board design. Finally, STMicroelectronics engineers imported the new design into Nexxim and re-ran the eye diagrams. The eye diagrams for the optimized design showed that the problems seen in the original eye diagrams had been corrected.

Based on a single global model that covered chips, packages, decoupling capacitors and the PCB, STMicroelectronics engineers were able to check signal and power integrity, and identify problems in both areas. They then made corrections and validated the optimized design. This method has reduced DDR system validation time by 50 to 66 percent and has become the standard workflow at STMicroelectronics.