OVERCOMING UNCERTAINTIES IN HIGH-SPEED COMMUNICATION CHANNELS

ANSYS HFSS helps verify the ability of cost-effective laminates to support communications speeds of 10 gigabits per second or greater.

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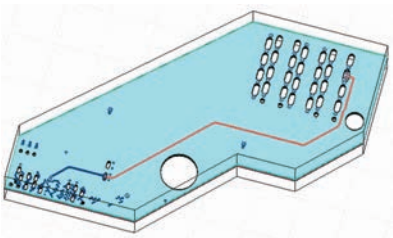
Each new generation of networking products delivers higher performance than the last — at equal or lower cost. Engineers tasked with designing high-speed communications channels for these products face a difficult challenge. The increased uncertainties involved in system performance at speeds of 10 Gb/s and higher encourage engineers to design for higher safety margins by choosing more sophisticated printed circuit board (PCB) laminate materials despite the higher costs. On the other hand, competitive pressures place a premium on the use of the most cost-effective materials and components, which may create uncertainties in product performance, possibly forcing a redesign at great expense after the hardware becomes available.

Engineers at Alcatel-Lucent Enterprise — a leading provider of products and innovations in Internet protocol (IP) and cloud networking, as well as ultra-broadband fixed and wireless access — addressed this challenge by using ANSYS HFSS to evaluate the performance of different materials and components in the early stages of the electronic design process. As an example, engineers extracted simulation channels from the post-layout database of two boards, concatenated them, and ran simulations in the frequency and time domains. They used

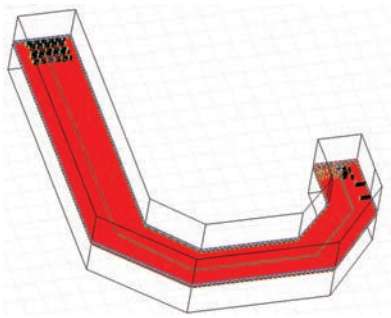
HFSS to determine the lowest-cost solution to reliably link integrated circuits (ICs) on two separate boards across a 12.5 Gb/s channel.

The channel links two boards, A and B, through an inter-board connector. During the initial concept design, relatively low-cost board materials were selected. Board A comprised an enhanced FR4 material that held the serializer-deserializer (SerDes) transmitter and a 3.3-inch differential channel that connected one IC to the connector. The channel started at the IC and extended about 0.5 inch on the top surface until it transitioned to layer 3 to reach its final destination at the connector. Board B comprised Megtron 4 material holding the SerDes receiver IC and an 11-inch differential channel that connected its IC to the connector.

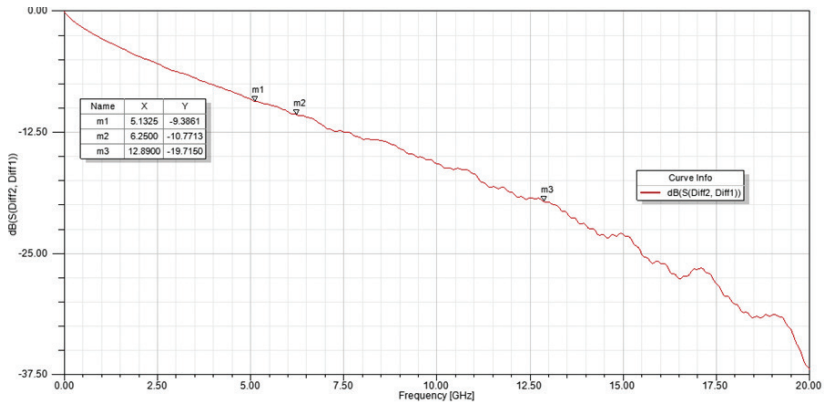
The project's simulation objective was to verify that a 12.5 Gb/s channel can reliably link two ICs located on two separate boards connected with a high-performance connector. The design specified that the frequency domain insertion loss (IL) must increase monotonically until its Nyquist frequency of 6.25 GHz without exceeding 20 dB, and the return loss (RL) must stay above 12 dB up to 6.25 GHz. In addition, the design needed to achieve stringent time-domain performance. The bit-error rate (BER) should be 10 to 22 or better after the signal has passed through the analog equalizer and decision-feedback equalization (DFE) filters located in the SerDes receiver IC.



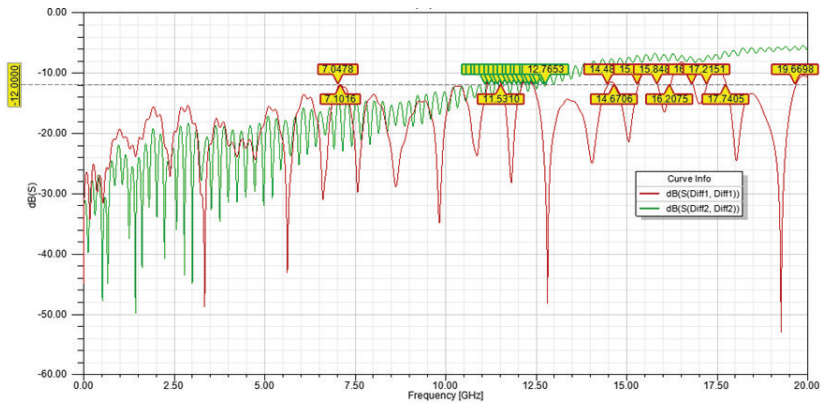
▲ Board A



▲ Board B



▲ Insertion loss simulation



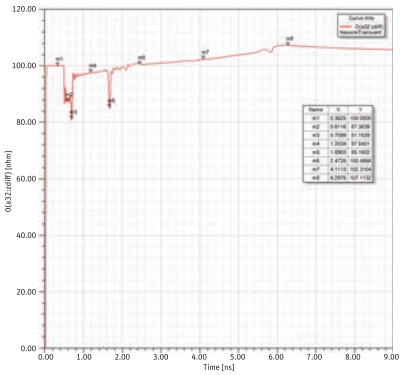
▲ Return loss simulation

FREQUENCY DOMAIN SIMULATION

Alcatel-Lucent engineers used ANSYS Designer and ANSYS HFSS to simulate this channel. The simulation started by building a frequency domain model in HFSS that was ported into Designer to analyze the structure performance in the time domain. This process provided more accurate results than the competitive approach of starting with a time-domain model. In Designer, engineers extracted the channel on each board from the post-layout database using the cutout subdesign function. They verified the stackup, edited the cutout to eliminate incidental shapes that extend the simulation time, and created the port excitations. Then, they ported the structure to HFSS to account for the copper surface roughness and to generate a higher-fidelity model.

Engineers then ran the frequency-domain simulation and verified that each board met the expected frequency-domain specifications. They generated a four-port S-parameter channel model of each board in HFSS. After creating a circuit schematic in ANSYS Designer, they imported the models of the two boards and the connector model provided by the manufacturer, and concatenated them to simulate the IL and the RL of the complete channel. The results showed that the IL was 10.7 dB and RL was above 12 dB up to 7 GHz. Both of these simulations met IL and RL requirements.

ANSYS HFSS 3-D LAYOUT
ansys.com/83layout



▲ TDR simulation

HFSS 3-D simulation confirmed with a high degree of certainty that the channel will operate properly and meet frequency- and time-domain specifications.

TIME-DOMAIN SIMULATION

Next, engineers created a circuit with a single instance of the concatenated channel and used the time-domain reflectometry (TDR) probe built into Designer to visualize the impedance profile of the channel under test. The impedance discontinuities are responsible for increased IL, RL and closure of the eye. The results showed the expected profile of a three-inch board, connector and 11-inch board. The simulation results also showed an impedance discontinuity on board A that represented the trace transitioning from the top to the inner layer in the layout.

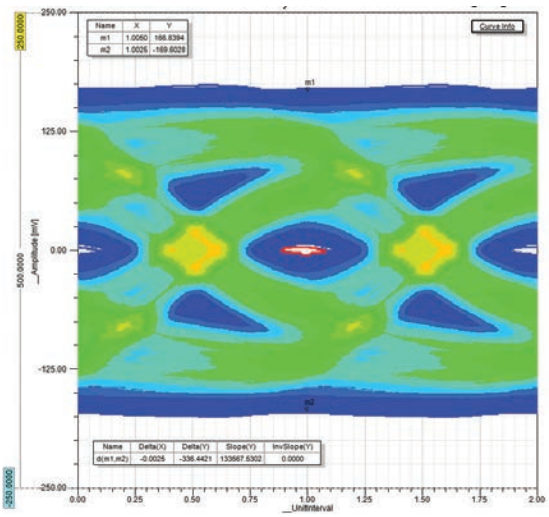
EYE DIAGRAM SIMULATION

Engineers then created a circuit to run the eye diagram (eye mask test) simulation. They used the same single instance of the four-port S-parameter model of the complete channel used in the TDR simulation and added the IBIS-AMI models of the transmit-and-receive SerDes provided by the IC manufacturer at each end of the channel. Using ANSYS Designer, the IBIS-AMI register settings were configured to maximize the opening of the eye.

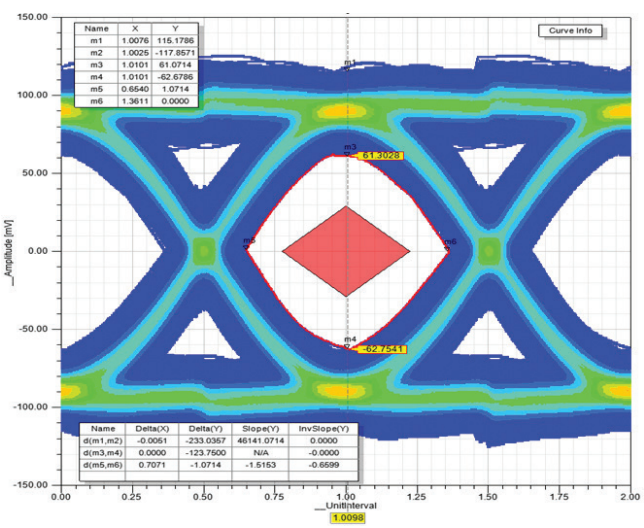
Engineers measured the eye diagram at the receiver IC after the built-in analog receiver and DFE filter. Even though the display showed a closed eye at the receiver IC pad, the continuous-time linear equalizer (CTLE) and DFE filters at the receiver opened the eye within the silicon. The filtered signal eye mask correlated to a BER better than 10 to 22. Therefore, the simulation results indicated that the channel was also compliant in the time domain.

Designer and HFSS's powerful combination of frequency- and time-domain analysis enabled Alcatel-Lucent engineers to remove the uncertainties of the trade-off between performance and cost. The HFSS 3-D simulation confirmed with a high degree of certainty that the channel will operate properly and meet frequency- and time-domain specifications. The results showed that a reliable product can be built with less expensive materials and connectors and will still exceed the BER objective. Engineers also verified that the channel meets the IL and RL frequency-domain specifications. As a result of this work, Alcatel-Lucent engineers were able to reduce PCB costs by 67 percent and achieve 5 percent savings in the overall cost of the system while avoiding the risk of expensive late-stage design changes that disrupt the project schedule.

Thanks to David Choe of ANSYS for his mentoring, great technical knowledge, familiarity with the tools, and patience while demonstrating the use of ANSYS Designer and ANSYS HFSS. Thanks also go to Michael Nisenson at ANSYS for his continuous and steadfast support.



▲ Simulated signal at receiver



▲ Eye mask simulation shows signal after RX equalizer and DFE.