NEAT AS A PIN

Rosenberger leverages mechanical and electrical simulation to provide a superior alternative to traditional spring pins for semiconductor testing.

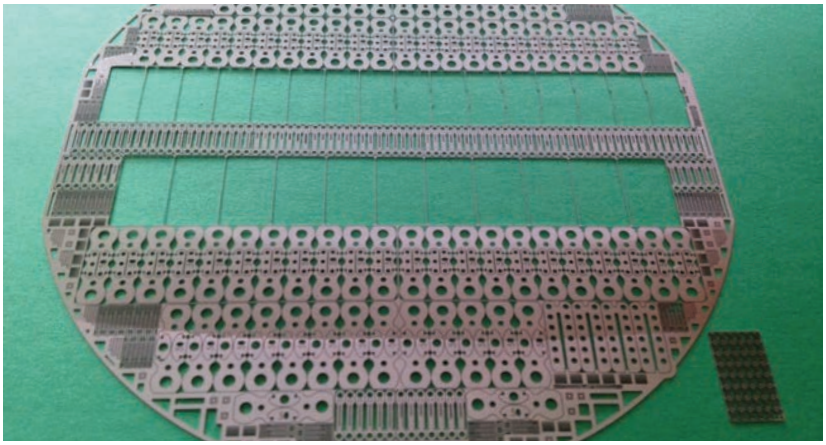
By Frank Schonig, Senior Member, Technical Staff; **Sandeep Sankararaman**, Electrical Engineer and **Steve Fahrner**, FEA Consultant, Rosenberger High Frequency Technology, Fridolfing, Germany.

Semiconductor manufacturers use automated test equipment (ATE) to verify that a specific device works before it is installed in the final product. Today's semiconductors are very complex devices performing many functions, and ATE usually tests all, or at least many, of these functions. ATE systems typically interface with a handler that places the semiconductor or device under test (DUT) on an interface test adaptor (ITA) with a socket that makes an electrical connection with connectors on the DUT. The many required connections between the DUT and the ATE are normally made with an array of spring pins or pogo pins consisting of high aspect ratio cylinders loaded with springs that generate force on the connectors as the DUT and socket are pressed together.

As the sizes of transistors and other features on semiconductors shrink, it is increasingly difficult to find space for all of the spring pins needed to make contact with electrical interconnects on the DUT, particularly when the DUT consists of integrated circuits on undiced wafers. But spring pins or pogo pins cannot be made much smaller with traditional manufacturing methods. Rosenberger High Frequency Technology has addressed this challenge by using the LIGA (based on the German acronym for lithography, electroplating and molding) process, which employs semiconductor manufacturing methods to accurately build tiny yet complex mechanisms — ones that are much smaller than the smallest interconnect produced by conventional methods. A monolithic-compliant interconnect (MCI) produced using LIGA can have features as small as 10µm wide, yet it has dozens of geometrical features that enhance its mechanical and electrical performance. The LIGA process allows mechanical engineers the freedom to design pins whose mechanical action is achieved without compromising electrical performance because it allows complex geometries in small volumes.

There are two types of LIGA processes: X-ray and ultraviolet (UV). In the X-ray LIGA process, a conductive seed layer is applied to a silicon wafer. Then a photoresist layer is applied with a spin coat process. The wafer is exposed to high-energy

Using simulation, Rosenberger engineers are able to optimize the MCI design from both mechanical and electrical standpoints.



▲ Individual MCIs superimposed on a coin

◀ MCIs and related components after removal from the wafer but before being separated into individual components

X-rays through a mask covered with X-ray absorbing materials in a pattern that is a negative of the cross-sectional geometries of the pins that are being manufactured. The photoresist is cured and the non-exposed photoresist is chemically removed, leaving a pattern of cavities over the surface of the wafer that matches the geometry of the MCIs to be built on the wafer. The wafer is plated using a plating bath. A negative charge is applied to the wafer that attracts metal ions to fill the cavities. The photoresist is removed with a plasma etch process, and the conductive seed layer is chemically removed to separate the parts from the wafer. The MCIs are finally coated with gold to improve electrical conductivity.

The variant of the X-ray LIGA process uses an ultraviolet (UV) light source rather than X-rays to expose a photoresist. X-ray LIGA offers higher accuracy and higher aspect ratios, while UV LIGA is more economical because it utilizes a relatively inexpensive ultraviolet light source.

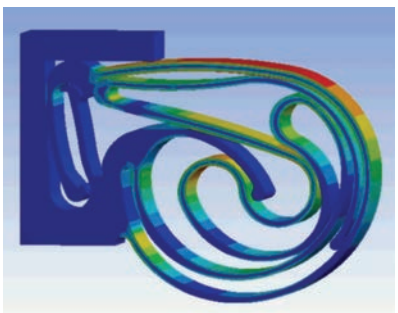
DIFFICULT DESIGN CHALLENGES

MCIs present extremely difficult design challenges from both mechanical and electrical perspectives. Mechanically, the objective is to minimize stress in the device to ensure that it will last for hundreds of thousands of contacts while delivering sufficient force at the contact interface — which is increased by maximizing the contact's ability to store strain energy (maximizing the force integrated over the distance of travel) — to ensure that electrical connectivity is achieved for each contact. From an electrical perspective, the objective is to ensure the integrity of signal transmission. The interconnects often are required to operate at very high frequencies during the testing process, increasing the electrical design challenge. These mechanical and electrical design requirements often conflict with one another. For example, additional material added to the interconnect to improve its fatigue performance might serve as an antenna that radiates a high-frequency signal traveling on the pin to neighboring pins or other circuitry in the ATE.

Rosenberger is a worldwide leading manufacturer of connector solutions in high-frequency and fiber optic technology fields. The company's engineers face dual challenges of developing designs that meet customers' demanding performance requirements and tight deadlines. Several dozen iterations typically are required to meet the goals for a single product, and Rosenberger designs scores of new products every year. Building and testing a prototype takes two to three months, with the majority of the time spent on the complex and expensive process of building the mask. The total time required to evaluate several dozen iterations using the build-and-test method is about six years, well beyond the normal time allotted for the design of a new product (six to eight weeks). Therefore, Rosenberger uses ANSYS Mechanical and ANSYS HFSS simulation tools in the ANSYS Workbench environment to iterate to a design that meets the customer's mechanical and electrical performance requirements while being robust enough to withstand manufacturing variation. The ability to perform the complete simulation process within a single environment reduces licensing, training and administration expenses; it also provides the potential to automatically optimize the design in the future for both electrical and mechanical properties.

MECHANICAL AND ELECTRICAL SIMULATION

The interconnect is designed as a 2-D part using one of several computer-aided design packages: AutoCad®, Ashlar Vellum™ software, SolidWorks® or Pro/ENGINEER®. It is then converted to a SolidWorks 3-D part to design the assembly consisting of multiple interconnects and their associated parts, such as connector blocks and printed circuit board (PCB) mounting hardware. When the geometric configuration of the contact has matured to the point that FEA analysis is required, the engineer imports a SolidWorks model into ANSYS Workbench and defines a static structural project. Most of the analysis is performed with the analysis type set to 2-D. Mechanical engineers modify the geometry, generating just enough pres-



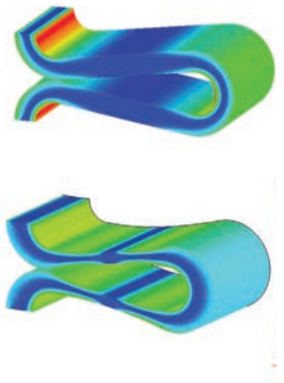
▲ Stress distribution of a portion of an MCI contact during cycling

sure to make electrical contact when the device is compressed, to minimize stress in the part. The final configurations are rerun using 3-D models and the 3-D analysis setting. The team then converts the deflected shapes (determined above) into 3-D CAD models of the deflected shape. For very simple models, the 3-D models can be output directly from Workbench. However, for more-complex models, the deflected geometry is exported as a vector graphics file. This file is used to create a SolidWorks model of the loaded/deflected part.

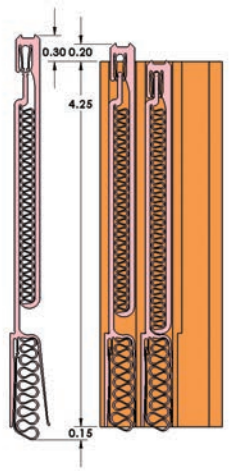
The 3-D model of the deflected shape is then loaded into HFSS for electrical/electromagnetic simulation. In HFSS, depending on the customer's application requirement — for example risetime, bandwidth or crosstalk — the engineer typically starts with a frequency sweep from DC to a suitable upper frequency. The engineer focuses on the S-parameters that describe how a signal on a given port scatters and exits on other ports, including reflection on the same port, transmission to connected ports and coupling to other ports. A typical target is an S11 return loss of –15 dB and an S21 performance of –1 dB. The HFSS output is typically exported to the ANSYS Designer circuit simulator that reads S-parameters to produce time-domain simulations used to evaluate the quality of a digital channel. The Rosenberger team often produces an eye diagram to provide instant visual data that engineers can use to check the signal integrity of a design. Adjacent signal paths are added to the simulation to evaluate the potential for crosstalk, and the composite response is checked against the customer specification.

The end result is that Rosenberger engineers are able to optimize the MCI design from both mechanical and electrical standpoints in a period of six to eight weeks. This saves a tremendous amount of time, since just one design iteration required three months in the past. The design freedom provided by the LIGA process along with using the multi-disciplinary tools provided by ANSYS has allowed Rosenberger to rapidly design products for diverse market segments.

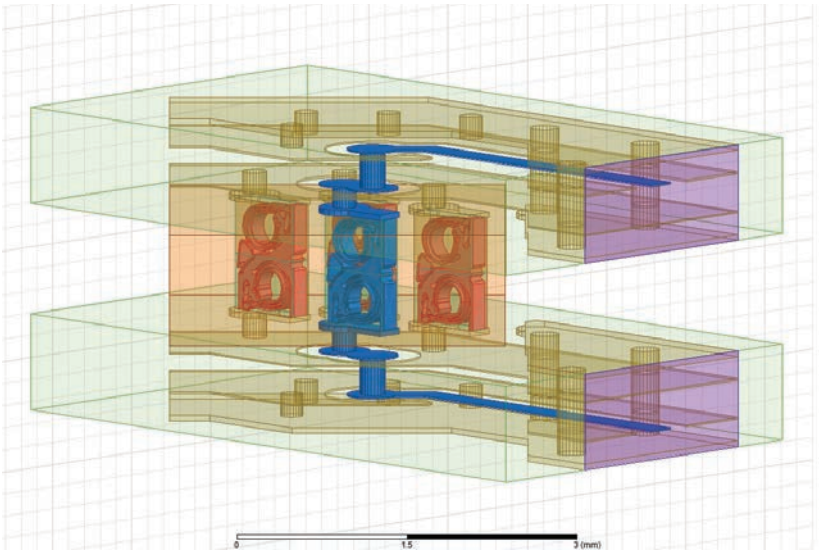
Company engineers are considering the potential for expanding the volume of the design space they can explore by utilizing design optimization tools to automate the process of iterating to an optimized design.



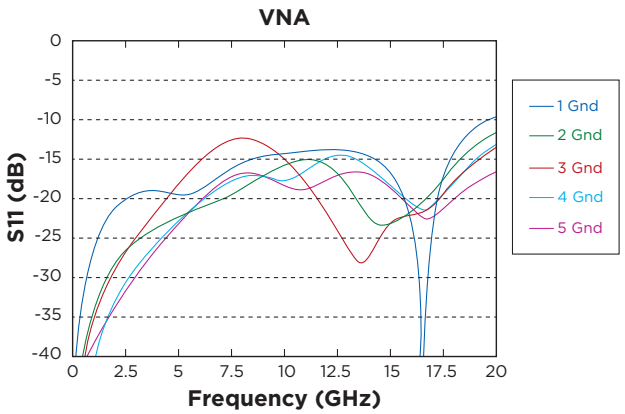
▲ Initial concept design of small section of MCI (top) and new design with modified taper (bottom) that increased force by 22 percent and reduced stress by 23 percent



▲ MCI (shown left to right) in as-manufactured, preloaded and full-travel positions



▲ ANSYS HFSS model



▲ S11 chart shows return loss of MCI.