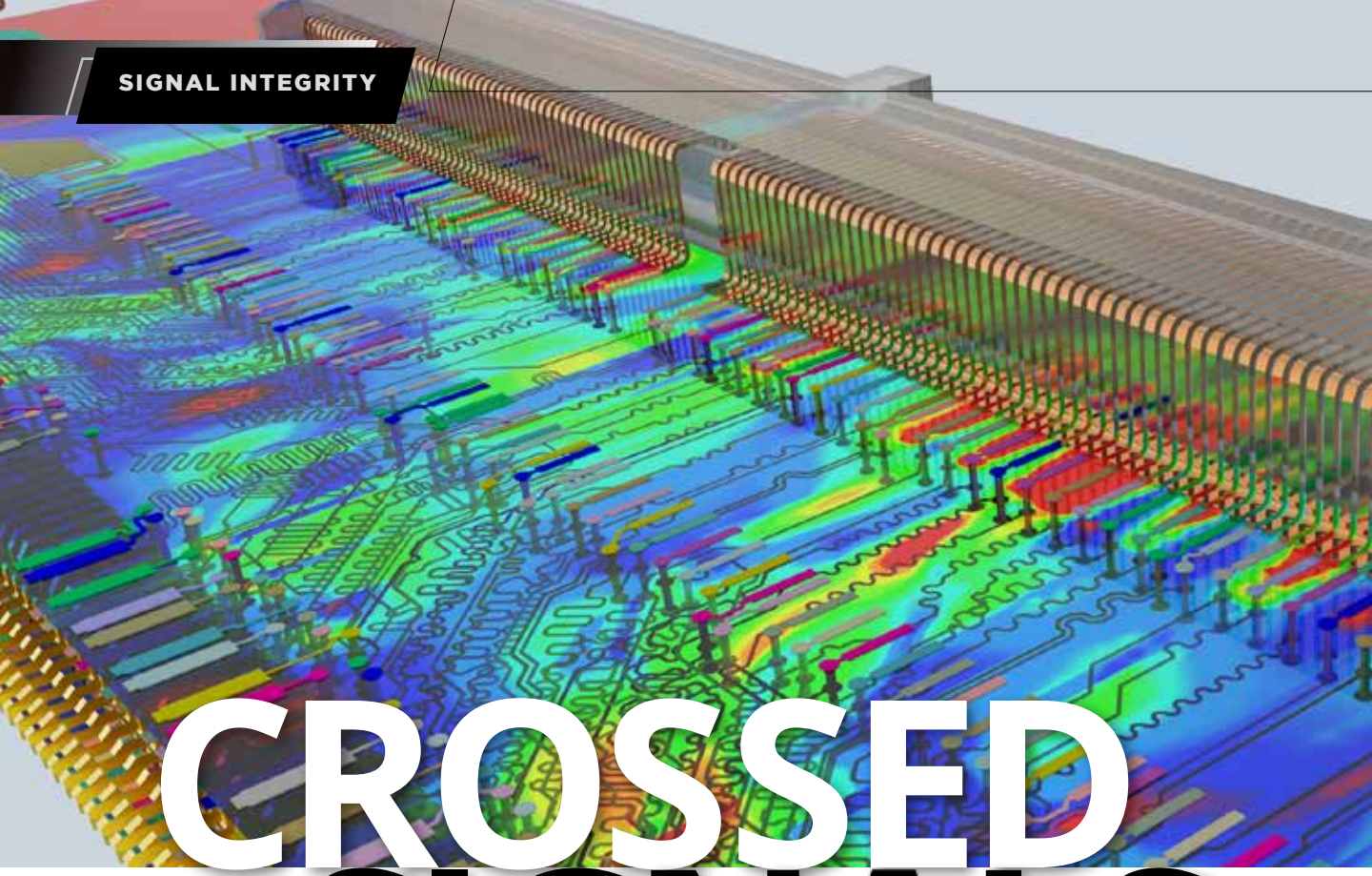
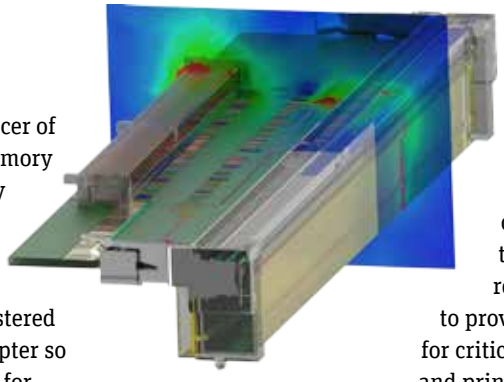


CROSSED SIGNALS

Smart Modular Technologies engineers leverage the ANSYS Electronics Desktop platform to reduce the time required to perform signal integrity analysis of a high-speed printed circuit from days to hours. By using unified electromagnetic, thermal and structural simulation, engineers developed a reliable adapter.

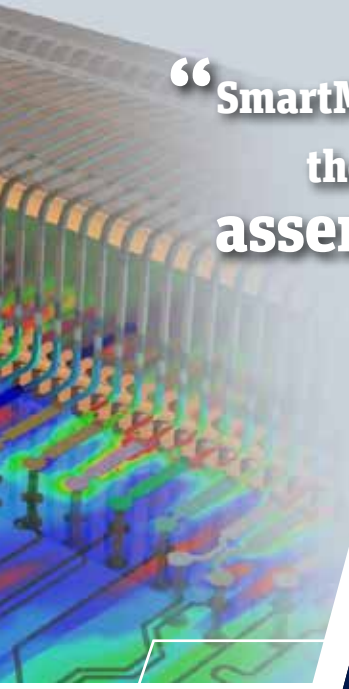
By **Fabio Bauman**, R&D Specialist, Smart Modular Technologies, Atibaia, Brazil



Electrical field on a cross section

Smart Modular Technologies (SmartM) is a leading producer of dynamic random-access memory (DRAM), flash and hybrid memory technologies. The company needed to develop a SO-DIMM-to-UDIMM (small outline dual in-line memory module to unregistered dual in-line memory module) adapter so that a test platform could be used for two types of modules. When installed, the first version of the adapter did not work, and engineers suspected a signal integrity problem. In the past, diagnosing the specific issue first required engineers to simulate the entire board in a 2.5-D EM simulator that can handle complex layouts, and then transfer the S-parameter result to a 3-D full-wave simulator to provide the high resolution needed for critical integrated circuit (IC) packages and printed circuit boards (PCBs).

Finally, the team would use S-parameter data from the combined simulation with a circuit simulator to run linear network analysis. This approach



> "SmartM engineers *reduced the time* to simulate the adapter by deploying the layout-driven **assembly workflow** introduced in **ANSYS Electronics Desktop.**"

SmartM SO-DIMM

SmartM UDIMM

was very time-consuming; the engineering team had to run two or three different software packages and several data export/import steps. This had to be repeated for each design iteration.

SmartM engineers reduced the time to simulate the adapter to hours by working with ANSYS channel partner ESSS to deploy the layout-driven assembly workflow introduced in ANSYS Electronics Desktop in ANSYS 18. The methodology combines several solvers, including ANSYS SIwave for complex PCBs, ANSYS HFSS for connectors and critical layout nets, and a circuit simulator in a unified platform, so that the S-parameter of the full channel can be extracted in an automated way. Simulation revealed crosstalk and impedance mismatches on three signal traces that compromised the eye diagram opening, jitter and bit error rates. SmartM engineers used these simulation results to determine the source of the problems and altered the board design to alleviate issues. They also leveraged ANSYS Icepak and ANSYS Mechanical to validate the board's thermal integrity and its ability to withstand thermal–mechanical stresses.

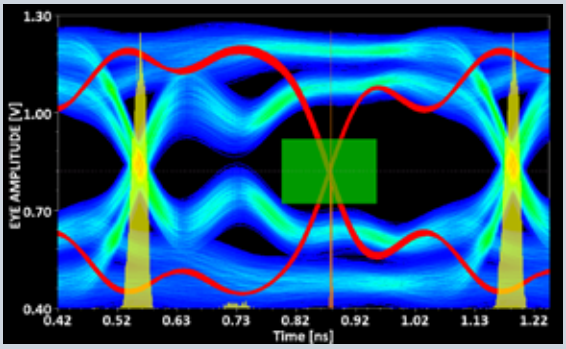
Tough Signal Integrity Problem

With high data rates and low voltage margins, signal integrity has become a pressing issue for printed circuit board designers. In this case, the board passed testing on an automated memory tester, providing a strong suspicion that signal integrity (and not memory) issues were at the root of the problem. The SIwave simulation showed crosstalk and impedance mismatches on several signal and clock traces. Next, engineers checked each byte lane, which showed closed eye diagrams.

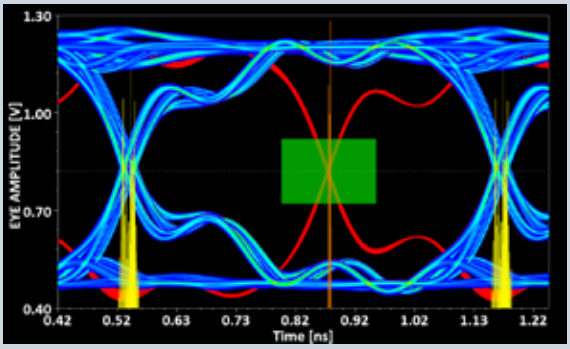
In the original design, the signal and clock layers were close to the PCB core with several split power and ground planes above and below them. SmartM engineers changed the stack-up to avoid problems such as impedance variations where traces cross the power–ground discontinuity. They repositioned the ground planes directly above and below the signal planes to improve the return path. Power was assigned to the top and bottom layers, and slow-speed and power nets were moved to the bottom layer, leaving only the critical memory data nets and clock signals on the internal signal layer. Engineers also experimented with layer thicknesses to optimize the impedance of the signal planes. Some traces were rerouted to avoid crosstalk between traces on the same layer.

Engineers ran impedance and crosstalk simulations again to check the effectiveness of the new design. The margins in the eye diagram were much larger than

Geometry Parameterization in SIwave
ansys.com/parameterization



Eye diagram of original design



The final design achieved a more opened eye, meeting the DDR4 specification.

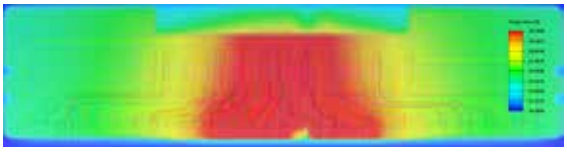
the original design, which indicated that the signal integrity problem had been solved. A DDR4 JEDEC JESD79-4 standard virtual compliance test confirmed that the new design exceeded DDR4 margins.

Thermal Integrity

Engineers then proceeded to analyze the thermal integrity of the new design. They calculated the DC currents, voltage drop and power in the PCB using SIwave, and the results were used to compute Joule heating. This heating is becoming an increasingly important source of thermal loading in PCBs as board sizes are reduced while power consumption stays the same or rises. The automated bi-directional workflow helped the team to export the board trace map and current density predictions to ANSYS Icepak. Icepak calculated the temperatures at every point in the board and automatically transferred this information back to the Electronics Desktop. SIwave updated the electrical properties of the DC solution based on the temperature field, and recalculated the board trace map and current density. The automatic iteration continued until the temperatures converged, indicating a temperature rise of only 12 C in the worst-case scenario.

Structural Durability

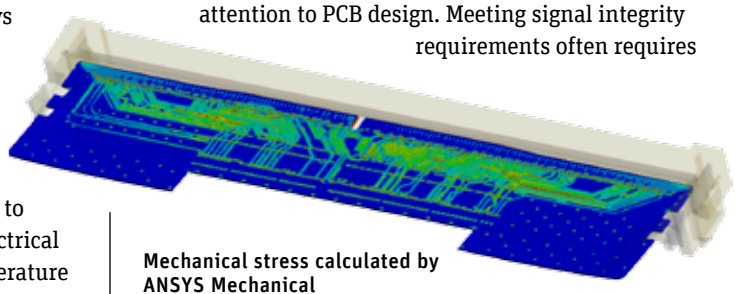
Engineers also considered the durability of the mechanical connection from the PCB to the SO-DIMM connector. They created a structural model using ANSYS SpaceClaim to read the ECAD geometry and



Temperature in the PCB calculated by ANSYS Icepak

convert it into solid geometry layers. They used ANSYS Mechanical to discretize the solid layers into a grid of elements. The details of the ECAD geometry were represented by assigning material properties to each element corresponding to the proportion of metal and dielectric appropriate for that element. The resulting finite element model provided accurate predictions of the stresses, strains and deformation generated by thermal or mechanical loading at any location on the board in a fraction of the time required to solve the fully detailed board geometry. The stress plot calculated by ANSYS Mechanical showed that the connector could perform reliably over its expected life.

The performance and reliability demands of modern electronic systems require that engineers pay close attention to PCB design. Meeting signal integrity requirements often requires



Mechanical stress calculated by ANSYS Mechanical

a very specific layout that can be extremely difficult to achieve with trial-and-error methods. Electromagnetic, thermal and structural simulation of PCBs provides a much faster approach to meeting today's high-speed interface standards. The integration of a wide range of multiphysics tools makes it possible, for the first time, to simulate the signal integrity, thermal integrity and mechanical integrity of a complete PCB in a time frame that is relevant to the design cycle in the early stages of the product development. In this project, SmartM was able to very quickly develop an internal solution customized to our engineering needs before this adapter hit the market, at 60 percent less cost than an adapter purchased from a supplier. At the same time, SmartM reduced the time and cost required for physical prototyping by 50 percent.

Smart Modular Technologies is supported by ANSYS Elite Channel Partner ESSS.