BOARD GAMES

ANSYS Electronics Desktop saves hundreds of thousands of dollars and months of time in the design of a high-speed printed circuit board.

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To support the vast amounts of data transfer required by the Internet of Things and Big Data requires high-speed networking technologies, such as 100 gigabit Ethernet. This creates enormous challenges for equipment suppliers. On-board, high-speed communication channels are now being pushed to 25–28 Gb/s and beyond — nearly double the state of the art about a year ago. As data rates increase, the bit period (the time allotted to send a bit) has shrunk to below 40 picoseconds. This is considerably less than the time required for the bit to travel from transmitter to receiver. The insertion loss incurred by the printed circuit board (PCB) materials increases with frequency, expanding the potential for eye closure (a reduced signal) in the channel due to physical losses and reflections. Achieving a reliable link under these conditions would be

ANSYS INTRODUCES NEW ELECTRONICS DESKTOP WITH 3-D EM COMPONENT LIBRARIES FOR NEXT-GENERATION WIRELESS INTEGRATION
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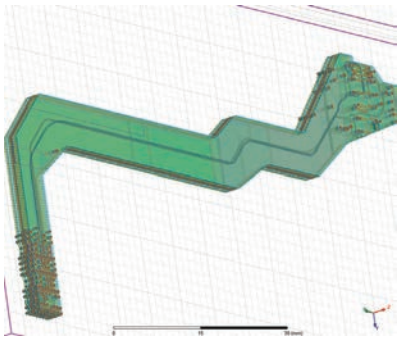
demanding, even if cost and time to market were not a concern. Yet, in today's cost-competitive environment, manufacturers cannot afford to use exotic, premium materials and components except when absolutely necessary.

HIGH-SPEED INTERCONNECT DESIGN CHALLENGES

Traditional methods leave designers with questions like whether a design will be functional and robust under all possible conditions; whether we should have chosen a more expensive board material; whether strip-line transmission lines or microstrip transmission lines will be needed to meet the design spec. Building a physical test prototype to assess just one design approach could cost more than $100,000 and take months to develop. At these high signaling rates, it is almost impossible to do any level of design, verification and test (DVT). Areas where a measurement can be taken on the board will result in a closed eye because testing cannot be performed at the end of the transmission line, which is deep inside the package and device. If designers only guess at the required changes for a re-spin, the whole expensive cycle begins anew and will likely be repeated. Several small networking equipment startup companies have gone out of business because they were unable to produce robust designs within time and cost constraints.

In stark contrast to this guesswork and rule-of-thumb approach, simulation brings confidence and science to the engineering process. The marriage of time domain and frequency domain simulations, during early design phases or even late in the development cycle, provides the deepest insight into whether or not an interface or channel will be robust. For example, a time-domain simulation might produce an eye diagram that shows that the channel works, but the frequency domain reveals a notch that is unexpected. By examining, through simulation, each of the circuit elements that comprise the system channel, it becomes possible to identify which aspect of the design (the vias, a differential pair too



▲ ANSYS HFSS 3-D layout of cutout section of one of 28 6-inch Gb channels

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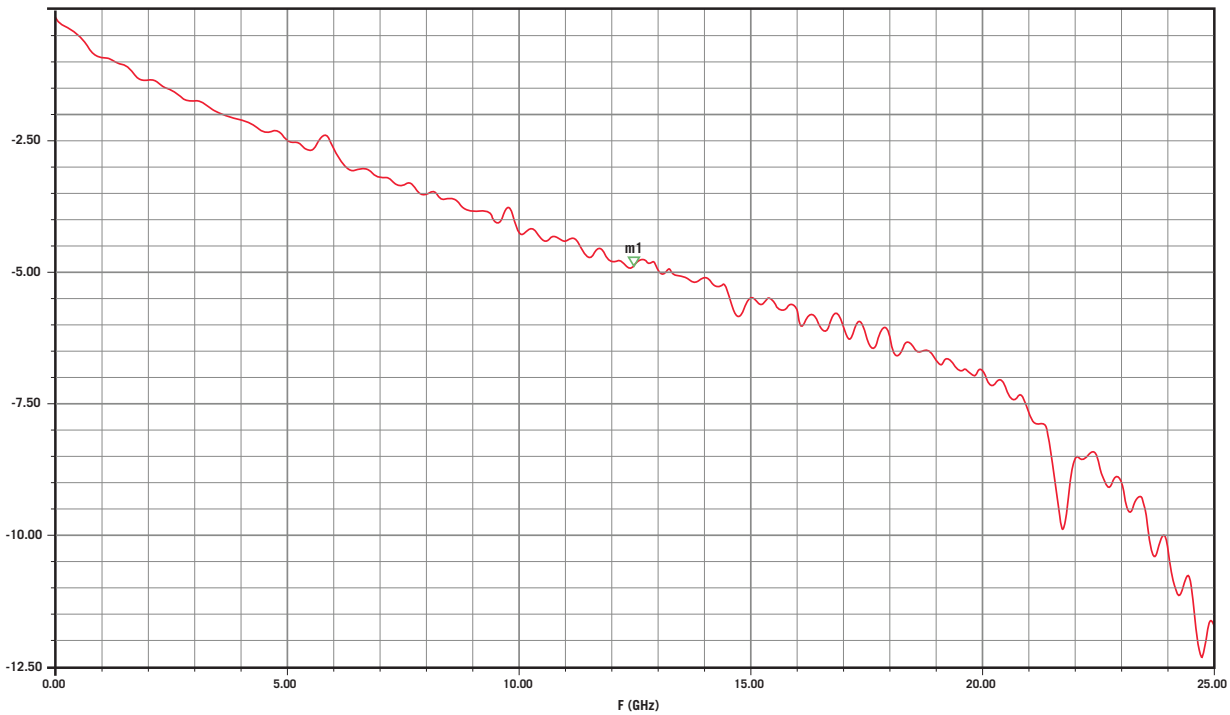
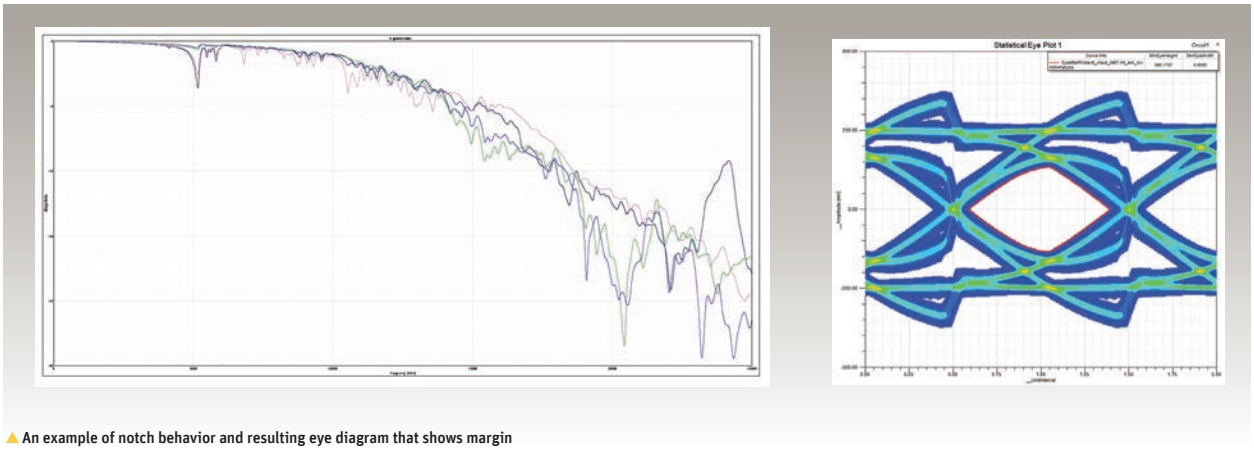


▲ ANSYS HFSS S21 insertion loss plot of the extracted channel



▲ An example of notch behavior and resulting eye diagram that shows margin

close to a ground void, a component placement issue or a material problem) is causing the notch.

100-GIGABIT ETHERNET NETWORKING PRODUCT

Interconnect Engineering Inc. is an independent consulting company with clients ranging from startups to Fortune 500 businesses. One of Interconnect Engineering's clients is a networking equipment supplier that builds multiple 100-gigabit Ethernet networking products. One particular design features four channel-bonded, 28 Gb/s links running bidirectionally from a ball grid array (BGA) device to a quad small-form-factor pluggable (QSFP) optical module. The risks involved in this design were increased because vendor-supplied guidelines and constraints were not

ANSYS Electronics Desktop integrates EM tools, circuit/system simulation, ECAD links and compliance reporting.

easily attainable based on the physical layout that the customer design supported. To avoid risking the company on a series of board spins that would have potentially cost hundreds of thousands of dollars — and taken months to complete — the supplier asked Interconnect Engineering to simulate the design prior to building a prototype.

While Interconnect Engineering Inc. has long used and supported ANSYS electronic design tools, this project provided the opportunity to put the new ANSYS Electronics Desktop to the test. This tool provided a major advantage in this application by reducing the amount of time required to analyze the design in both the time and the frequency domains. The Electronics Desktop integrates EM tools, circuit/system simulation, ECAD links and

ANSYS HFSS 3-D COMPONENTS
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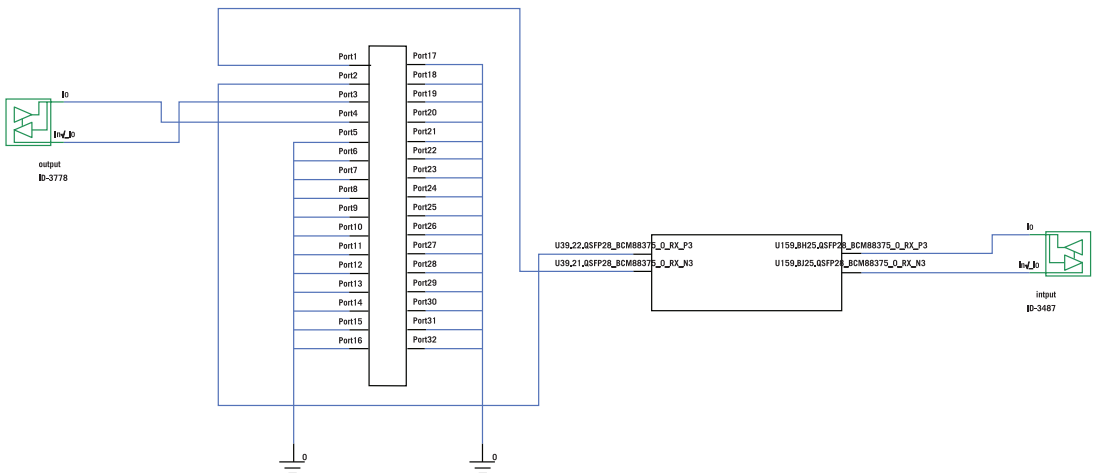
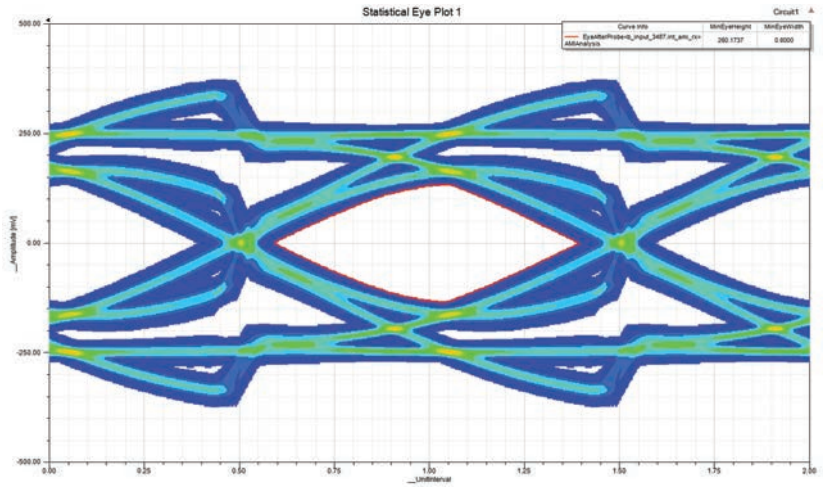


▲ IBIS-AMI schematic of the 28 Gb interface shown in the circuit simulator



▲ Statistical eye diagram plot of the 28 Gb interface shown in the circuit simulator

The networking supplier saved hundreds of thousands of dollars and months of time that potentially would have been required to develop a working product without simulation.

compliance reporting. This new technology delivers a single desktop for ANSYS HFSS, HFSS 3D Layout, HFSS-IE, Q3D Extractor and HFSS Planar EM circuit and system simulation design types. Users can insert HF/SI analyses into projects that co-exist, with drag-and-drop dynamic links between electromagnetic and circuit simulations for simple problem setup and reliable performance. Working within a single graphical user interface, rather than moving back and forth between several different programs, eliminates the need to export data from one program to another. For example, users can insert S-parameter elements or IBIS-AMI models into a circuit simulation with simple import features. Overall, the Electronics Desktop provides significant efficiency gains and ease-of-use for solving complex problems.

FREQUENCY DOMAIN SIMULATION

In this project, the network equipment supplier provided Interconnect Engineering with the PCB design in Allegro .brd file format. An engineer imported the databases into ANSYS Electronics Desktop, extracted the relevant channels using the cutout subdesign function, and selected the traces from the silicon device to the optical module. The engineer created port excitations based on component specifications then set up solder-ball models for the silicon device and surface roughness models for the traces to add fidelity and accuracy. Engineers then ran frequency domain simulations with ANSYS HFSS and generated the S-parameter results for each of the multiple iterations. The simulations took about three days to run on multiple 24-core machines, as the area was quite large for the solvers to mesh.

The engineer modified the via characteristics and anti-pad structures and re-arranged the PCB layers to address some potential issues. The engineer then went through several iterations until a design was found that met the insertion loss (IL) and return loss (RL) specifications. He considered alternative board materials and identified the least-expensive material that would comfortably meet IL and RL specs. Overall, Interconnect Engineering identified areas in which corners could be safely cut to reduce manufacturing costs, along with areas in which money needed to be spent, such as backdrilling to ensure a robust design.

TIME DOMAIN SIMULATION

IBIS-AMI models for the BGA interface device and optical transceiver module were also acquired. These models were imported into ANSYS Electronics Desktop. Engineers then performed time domain simulations by creating a circuit simulation environment using one instance of the several four-port S-parameter models of the complete channel generated in the frequency domain. The eye diagram showed problems in one channel, so the engineer reconfigured transmitter and receiver settings, including pre-emphasis, equalization, output amplitude, process case and voltage settings, to maximize the opening of the eye. When simulations were complete, the eye correlated to a bit error rate of better than 1×10^{-12} (less than one error in a trillion bits), indicating that the channel was compliant in the time domain. Finally, the engineer reviewed the frequency domain to make sure that the design changes, based on the time domain simulations, did not have any adverse effects.

The entire project was completed in about four weeks. During this time, Interconnect Engineering investigated dozens of potential solutions. The company recommended a design that provided sufficient positive margin to ensure that the channel will work under any foreseeable circumstances, while keeping manufacturing costs at the lowest practical levels. The network equipment supplier built the prototype based on the simulation results, and it worked as predicted. The result was that the networking supplier saved hundreds of thousands of dollars and months of time that potentially would have been required to develop a working product without simulation. This vendor also kept manufacturing costs at or near the lowest possible levels and saved customer relationships by meeting product time-to-market goals.