Speeding to a Solution

ANSYS HPC helps a consulting firm evaluate high-fidelity models with rapid turnaround.

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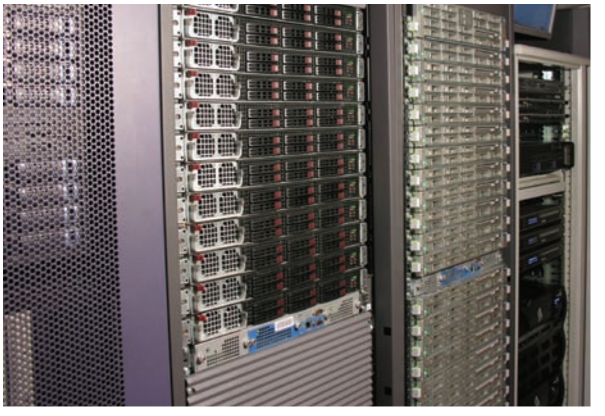
An automotive electronics supplier contracted with MicroConsult GmbH, a computer-aided engineering services company, to help develop a better understanding of why solder joints were failing in an electronic control unit (ECU) [1].

The solder joints that connect the integrated circuit (IC) to the printed circuit board (PCB) are subject to failure due to mechanical stresses during thermal cycling caused primarily by thermal mismatch. The assembly process and mechanical tolerances during manufacturing impose additional mechanical stresses on the joints. Restriction of Hazardous Substances (ROHS) legislation requires only lead-free materials to be used for solder joints. Consequently, the available knowledge about the damage behavior of leaded solder joints needed to be revised. Reliability testing can take 1,000 to 2,000 hours for typical test scenarios, so it is crucial to use simulation to gain insight into the underlying dependencies.

MicroConsult engineers performed a thermal simulation on the ECU, then used the data as an input for a mechanical simulation of the ECU; they subsequently applied the temperatures and displacements to a submodel of the IC for a solder creep–strain analysis. When originally solved with ANSYS Mechanical 11.0, the analysis required two weeks per design iteration. Improved high-performance computing (HPC) hardware and advances in subsequent ANSYS development reduced the time to solve the model to half a day. The reduction in simulation time has made it possible to use more complex, more accurate models and to evaluate many more design concepts.

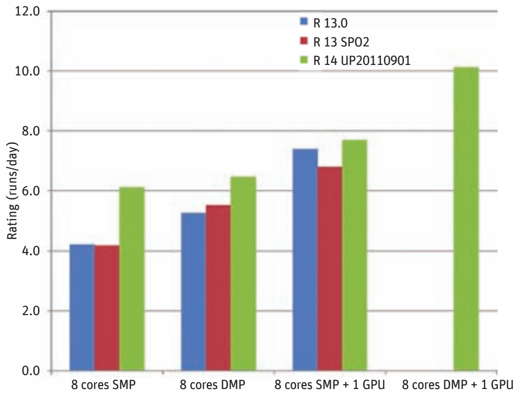


HPC hardware recently installed at MicroConsult

MicroConsult created a system-level model of the ECU together with the PCB and IC. During reliability testing of the hardware — thermal cycling in an oven — the temperature was recorded for a number of measurement points

		ANSYS 11.0	ANSYS 12.0	ANSYS 12.1	ANSYS 13.0 SP02	R&D for ANSYS 14.0	
Thermal (full model) 3M DOF	Time	4 hours	4 hours	4 hours	4 hours	1 hour	0.8 hour
	Cores	8				8 + 1 GPU	32
Thermomechanical Simulation (full model) 7.8M DOF	Time	~ 5.5 days	34.3 hours	12.5 hours	9.9 hours	7.5 hours	
	Iterations	163	164	195	195	195	
	Cores	8	20	64	64	128	
Interpolation of Boundary Conditions	Time	37 hours	37 hours	37 hours	0.2 hour	0.2 hour	
	Load Steps	16	16	16	Improved algorithm	16	
Submodel: Creep–Strain Analysis 5.5M DOF	Time	~ 5.5 days	38.5 hours	8.5 hours	6.1 hours	5.9 hours	4.2 hours
	Iterations	492	492	492	488	498	498
	Cores	18	16	76	128	64 + 8 GPU	256
Total Time		2 weeks	5 days	2 days	1 day	0.5 day	

All runs with SMP Sparse or DSPARSE solver
Hardware 12.0: dual X5460 (3.16 GHz Harpertown Xeon) 64GB RAM per node
Hardware 12.1 + 13.0: dual X4170 (2.93 GHz Nehalem Xeon) 72GB RAM per node
ANSYS 14.0 creep runs with NROPT, crpl + DDOPT, metis
ANSYS 12.0 to 14.0 runs with DDR Infiniband® interconnect



This graph illustrates the progress during 2011 from adding GPU support for shared memory solvers (SMP) with ANSYS 13.0 to using distributed solvers (DMP) with GPUs for ANSYS 14.0.

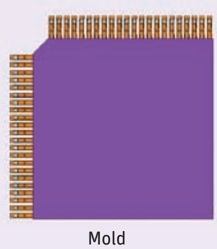
on the PCB as a function of time during each test cycle. After the parameters were tuned, the simulation provided the temperature distribution, most importantly near the IC's corners where the PCB solder joints are located, with negligible error.

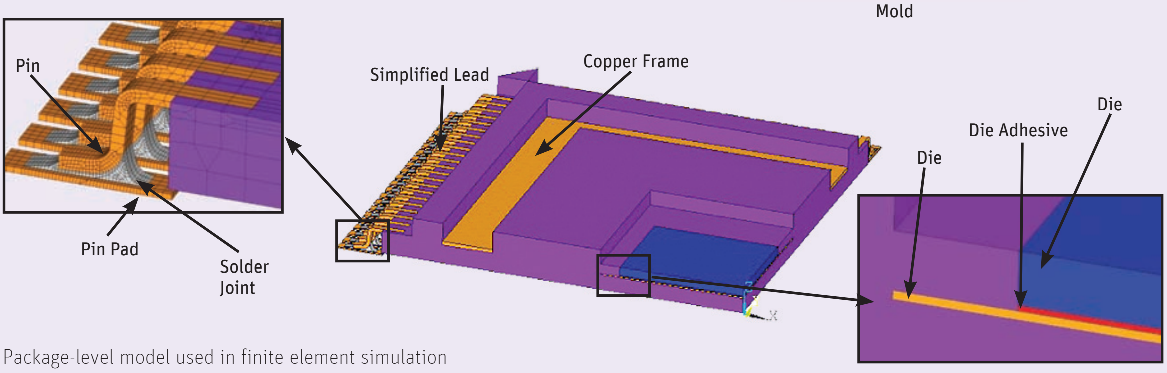
The results of the transient thermal analysis were used as input to a structural simulation of the entire ECU. ANSYS Mechanical results showed the mechanical strain on the PCB, which was compared to experimental measurements at 15 different PCB locations using strain gauges. The transient displacements of nodes at the cut boundary of the submodel — which consisted of the IC and a section of the underlying PCB — and the temperature field for this region were used as boundary conditions for the creep simulation. A creep–strain analysis of the submodel correctly predicted the location of the most damaged solder joints in the IC corners. Most important is that the simulation revealed that differences in the failure pattern for the four corners of the IC package are due to the influence of the ECU.

MicroConsult has been involved in many similar applications in which simulation has provided extremely valuable input to the design process yet the amount of time required for each simulation was a limiting factor. Despite being a small company with five employees, MicroConsult has aggressively invested in HPC technology. The first step into number crunching was in 2004 with the purchase of a quad-socket Opteron™ system with four cores and 16 GB RAM. At that time, the use of ANSYS shared memory parallel (SMP) solvers was dominant. Since then, ANSYS has invested in software development focused on HPC performance, and these improvements have dramatically reduced the time required to solve simulations like this solder fatigue analysis. For MicroConsult to run such studies efficiently, the investment in HPC cluster technology was key.

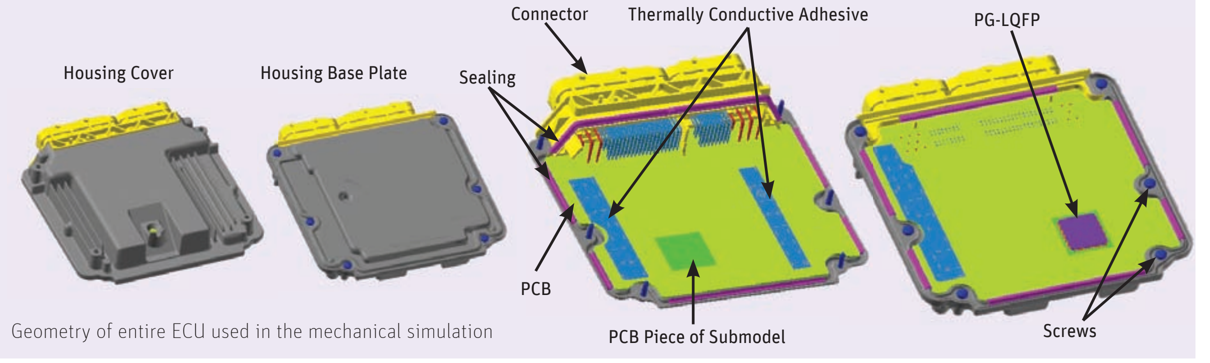
The first solder creep simulation that included ECU effects was performed in 2008 using ANSYS 11.0. Distributed computing was relatively new in that ANSYS release, and not all physical models were supported. It took about four hours for the system-level thermal simulation to run on a compute node with dual Intel® Xeon® 5460 processors. The subsequent structural simulation running on the same hardware added 5.5 days. Interpolating boundary conditions from the system-level to the package-level model took 37 hours. Finally, after another 5.5 days, the results of the creep–strain analysis for the submodel were available. The package-level model was the first to use more than a single compute node. MicroConsult combined 16 cores on two compute nodes and used a distributed sparse solver. The total run time of approximately two weeks limited the value of simulation in the design process.

Device Component	Dimensions of the Entire Geometry (mm)
Mold	24 x 24 x 1.36
Die	8.2 x 6.6 x 0.29
Die Adhesive	8.2 x 6.6 x 0.03
Die Pad	9.5 x 9.5 x 0.08



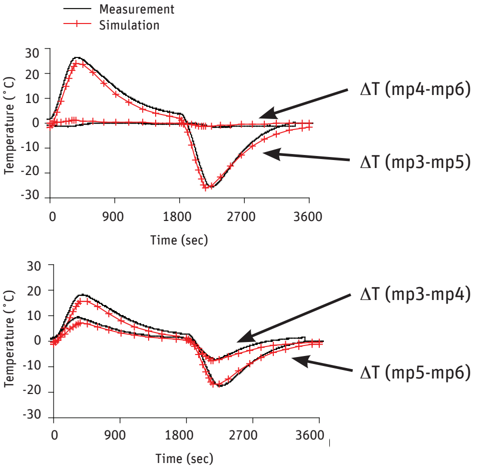


Package-level model used in finite element simulation

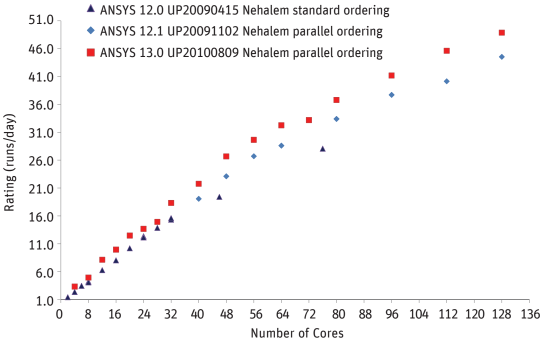


Geometry of entire ECU used in the mechanical simulation

In 2009, MicroConsult upgraded to ANSYS 12.0, which provided optimized parallel computing performance. With this software release running on a cluster, total solution time was reduced to five days. The Intel® Nehalem processor also became available in 2009. It brought a substantial increase in memory bandwidth that helped improve scaling for higher core counts. In fall of the same year, ANSYS introduced HPC Packs with ANSYS 12.1. This licensing option encourages the use of large-scale HPC, making it possible for MicroConsult to increase the cluster core count to 80 cores. With Sun Microsystems Sun Fire™ X4170 compute nodes with dual Intel Xeon 5570 processors, the runtime for the ECU mechanical simulation was reduced to 12.5 hours on 64 cores, and the creep–strain analysis could be done in 8.5 hours. Total solution time was reduced to two days.



Comparison between simulation and physical testing results of temperatures at points on the PCB near the IC corners



Scaling improvement in ANSYS Mechanical 12.0, 12.1 and 13.0

Finally, ANSYS Mechanical 13.0 provided an improved algorithm that reduced the time required for interpolating boundary conditions to 12 minutes instead of 37 hours, along with new creep–strain capabilities that reduced analysis time to 5.7 hours. The complete sequence of simulations can now be performed in one day, more than an order of magnitude faster than what was required just three years ago.

Further improvements are on the way. In 2011, MicroConsult added eight NVIDIA® M2070 Tesla™ Accelerators (GPUs) and 12 Supermicro® 1026GT compute nodes. The equation solvers offload highly parallel number crunching algorithms from the CPU cores onto GPUs for a substantial increase in speed.

MicroConsult recently tested a pre-release version of ANSYS 14.0 (UP20110901), which also enables the use of GPUs for distributed solvers, on this same model. The GPU-accelerated run (eight nodes, 64 cores, eight GPUs) for the submodel delivers the same performance as ANSYS 13.0 service pack 2 with half the number of compute nodes and half the number of cores. This substantially reduces energy consumption.

To further improve performance, all available cores were combined in a cluster with 256 cores. Doubling the number of cores reduced the total runtime by 31 percent for the submodel run. The speedup was less than linear because performance on this model with this hardware levels off at 128 cores. Running the job on 256 cores is not the most efficient use of resources. But this method can be invaluable when facing a tight deadline in which overall throughput is more important than scaling efficiency.

Over the last several years, improvements in HPC hardware and ANSYS software have dramatically reduced the time required to solve large and complex design problems. In the example detailed above, the amount of time required to perform fatigue analysis on solder joints was reduced by more than an order of magnitude. HPC is also about increasing analysis accuracy by using larger and more complex models. Alternatively, the same hardware could be dedicated to solve a large number of smaller problems simultaneously — thus opening the door to design optimization. ■

Reference

[1] Schafet, N.; Lemm, C.; Becker, U.; Güttler, H.; Schmidt, P. *Development of a Submodel Technique for the Simulation of Solder Joint Fatigue of Electronic Devices Mounted within an Assembled ECU*. Proceedings of EuroSimE 2009, pp. 253–260, Delft, Netherlands, April 2009.