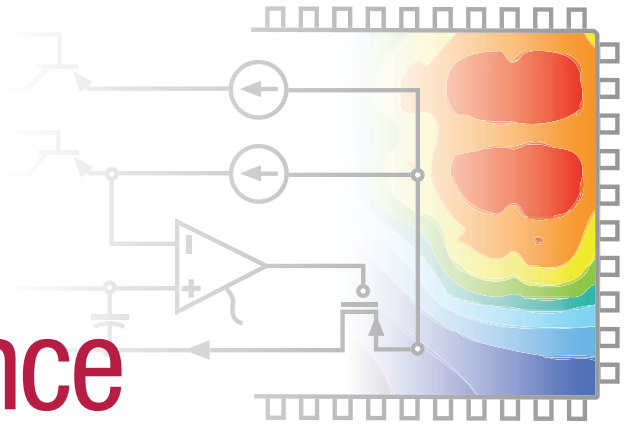


Low Power, High Performance

The acquisition of Apache increases ANSYS capabilities for designing low-power electronics devices while satisfying ever-increasing performance requirements.

By Aveek Sarkar, Vice President, Product Engineering and Support, Apache Design, Inc.

When Andrew Yang founded Apache Design Solutions in 2001 along with three researchers from HP Labs, he realized that as chip design engineers strived to meet the goal of increased device miniaturization (in accordance with Moore's Law, which states that the number of transistors and resistors on a chip doubles every 18 months), they would eventually hit stumbling blocks. Success in the end would depend on how well chip design engineers managed power consumption, power delivery and power density of their designs. It would also depend on how well they navigated the fragmented, silo-based electronic design ecosystem and worked cohesively to achieve competitive differentiation and cost reduction for their end products.

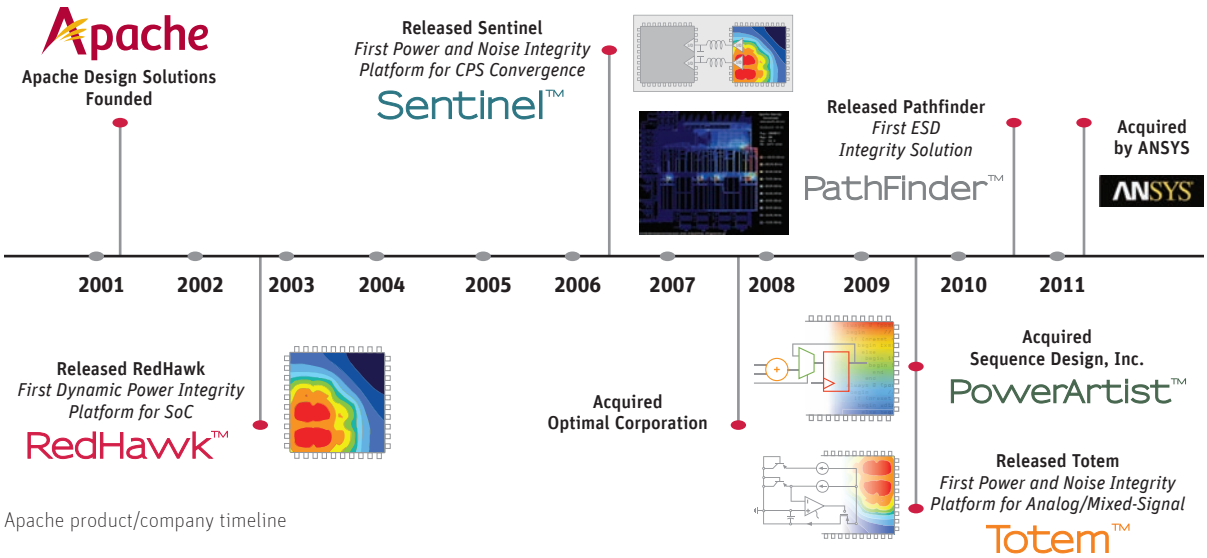
As engineering teams struggled to control power consumption in smartphone, tablet and hand-held devices, they used various architectural and circuit techniques, including reduced voltage supply. These techniques made circuits more vulnerable to fluctuations and anomalies, either during manufacturing or operation. Before the release of Apache's first (and flagship) product, RedHawk, in 2003, chip design engineers relied on approximations and DC (static) analysis methods that are insufficient for predicting fluctuations coming from the interaction of the chip with its package and board. Due to the lack of existing solutions and associated methodologies, chip, package and system design teams worked in isolation, typically resulting in overdesign, increased costs, or failures leading to product delays.

The launch of RedHawk addressed several of these issues, providing the industry with its first dynamic power noise simulation technology. For the first time, chip designers could simulate their entire design, along with the package and board, and predict its operation prior to manufacturing the parts. Apache's RedHawk introduced the industry to several key technologies that have become increasingly relevant, advances that are still unmatched more than 10 years later. These technologies, several of them patented, include:

- Extraction of inductance for on-chip power/ground interconnects, in addition to their resistive and capacitive elements
- Linear model creation of on-chip MOSFET devices through the use of Apache Power Models
- Automatic generation of on-chip vectors using a VectorLess™ approach
- Simultaneous analysis of multiple-voltage domains handling billion-plus node matrices and considering various operating modes on the chip such as power up, power down, and so on.

ANSYS simulation technologies address complex multiphysics challenges and enable Simulation-Driven Product Development. As semiconductor devices pervade every aspect of our lives, in cars, smartphones and smart-meters, their impact on the end systems (and vice versa) is becoming a key design challenge for our customers. The combination of Apache's chip-level power, thermal, signal and EMI modeling solutions, along with ANSYS package and system electromagnetic, thermal/fluids and mechanical simulation platforms, will enable faster convergence for the next generation of low-power, energy-efficient designs. Together with our joint teams, I look forward to solving our customers' design challenges, such as those associated with high-speed signal transmission, stacked-die design integration, and automotive and mission-critical electronic system reliability validation. We remain committed to our customers' success by providing consistent support and delivering continuous technology innovation in all our products and platforms.

Andrew Yang
President
Apache Design, Inc.



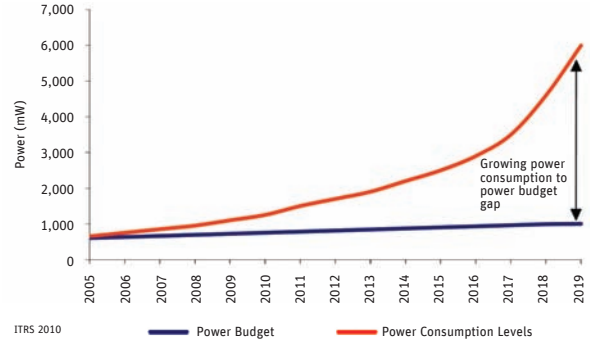
Apache product/company timeline

In its debut year, RedHawk received *EDN* magazine's Innovation of the Year Award (2003). RedHawk's first-in-class technologies, built on best-in-class extraction and solver engines, has led to its adoption as the sign-off solution of choice by electronic system designers around the world for power noise simulation and design optimization. To round out the portfolio, Totem software was launched to meet the distinct needs of analog, IP, memory and custom-circuit design engineers for power noise and reliability analysis.

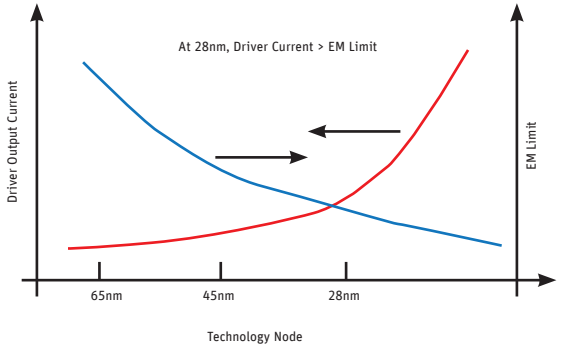
The introductions of Chip Power Model (CPM) technology and the Sentinel product family in 2006 were seminal events in Apache's history. For the first time, chip designers could create compact SPICE-compatible models of their chips that preserved time and frequency domain electrical characteristics of the chip layout. This model soon became the currency for the exchange of power data enabling chip-aware package and system analysis. For this industry contribution, Apache again received *EDN* magazine's Innovation of the Year Award (2006).

The success of smart hand-held devices depended on how efficiently designers could squeeze increasing functionality within much smaller form factors while managing to meet the end device's power budget. Apache's acquisition of Sequence Design in 2009, and the introduction of the PowerArtist platform, addressed chip designers' growing need to simulate designs very early during the design phase, when architectural definitions are created using register transfer level (RTL) descriptions. PowerArtist enables accurate and predictive RTL-based power analysis and helps to identify power bugs and cases of wasted power consumption in the design. This simulation-driven design-for-power methodology allows engineers to address the growing gap between device power consumption and the maximum allowed power in end electronics systems.

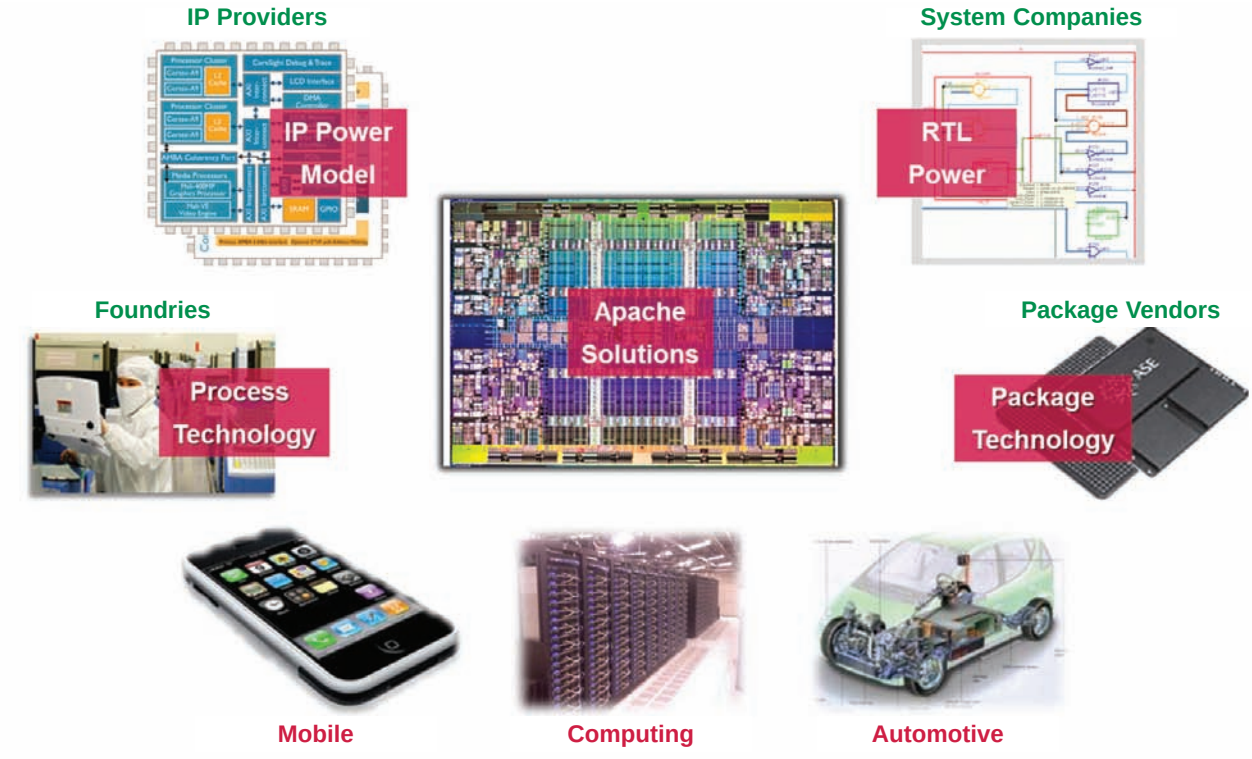
Increasing functionality requirements in smaller form factors have accelerated the adoption and use of advanced technology nodes such as 28 nanometer (nm), or even 22nm. The logic operations performed in a chip result in a flow of current in various interconnects on the chip. But the wires and vias fabricated using advanced technology nodes cannot sustain increased current levels and are at risk for field failures. Additionally, MOS devices and on-chip interconnects are increasingly susceptible to failures from high levels of current flow resulting from an electrostatic



The growing gap between power consumption in electronic systems and maximum-allowed power budget



Increasing divergence between current flowing in wires versus their ability to handle such current levels



The Apache simulation ecosystem brings semiconductor foundry, IP providers, system-on-chip (SoC) design houses, package vendors and system integrators together.

discharge (ESD) event. To address this growing design challenge, Apache introduced PathFinder, the industry's first full-chip-level, package-aware ESD integrity simulation and analysis platform. PathFinder enables designers to predict and address ESD-induced failure they would otherwise not be able to identify until very late in the product design cycle. Apache's PathFinder received *EDN* magazine's Innovation of the Year Award (2010).

As a company, Apache's revenue increased three times from 2006 to 2010, underscoring the strong adoption of its products and technologies by semiconductor and system design companies worldwide. Apache's achievements were recognized by Deloitte Technology's Fast 50 Award in 2008 as being among the top 15 fastest-growing software and information technology companies in Silicon Valley. The following year, Apache received Deloitte's 2009 Technology Fast 500 Award, honored as one of the fastest-growing technology companies in North America.

Apache employs a significant number of R&D and application engineering personnel dedicated to solving power noise and reliability challenges for chip–package–system designs. The R&D team focuses on consistently delivering first-in-class technologies and best-in-class engines to meet the capacity, performance and accuracy requirements that customers (which include the top 20 semiconductor companies, as measured by revenue in 2010 according to iSuppli) demand.

Apache's innovative product platforms create an analysis environment that brings together the disparate design teams that make up the ecosystem delivering today's electronic systems. These product platforms create user-friendly, compact models that enable data sharing and integrated design flows, fostering closer collaboration among design teams — such as between automotive or communications system companies and their IC suppliers, or IC design firms and their foundry or ASIC manufacturing partners.

Apache filed for an initial public offering under the symbol APAD in March 2011. On June 30, 2011, ANSYS, Inc. signed a definitive agreement to acquire Apache, and on August 1, Apache Design, Inc. became a wholly-owned subsidiary of ANSYS. The arrangement brings together best-in-class products that drive the ANSYS system vision for integrated circuits, electronic packages and printed circuit boards. The complementary combination is expected to accelerate development and delivery of new and innovative products to the marketplace while lowering design and engineering costs for customers. ■