Avoiding Excess Heat in TSV-Based 3-D IC Designs

Engineers use coupled simulation tools to resolve thermal issues at through-silicon vias (TSVs) early in development of high-density 3-D IC modules.

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One of the hottest trends in electronics is the growing use of 3-D integrated circuit (IC) designs in which multiple ICs are stacked in vertical layers, creating a high-density circuit module that packs significant functionality into a relatively small footprint at a reduced cost. Layers are interconnected by through-silicon vias (TSVs), in which fine wires transfer signals and power. In this way, conductor paths through the 3-D IC device can be extremely short (a fraction of a millimeter), leading to much faster operation compared to conductors that are routed down through the package, across a board substrate and then back up through another package.

Because of the close packing of 3-D ICs, thermal issues are a top priority — especially at TSVs where electrical currents are concentrated and holes in the silicon may be mechanically stressed by thermal gradients and structural loading. To identify potential problems early in design, an analysis can be performed using a combination of commercially available tools: GemPackage™ for model construction, SIwave software for DC analysis and ANSYS Icepak technology for thermal analysis. Furthermore, the process could be extended to easily study signal integrity/power integrity (SI/PI) issues because the same ANF file can be entered into ANSYS SI/PI tools, including SIwave, TPA, HFSS and Q3D Extractor (Figure 1).

GemPackage is a software tool for studying the physical feasibility of system-in-package (SiP) devices:

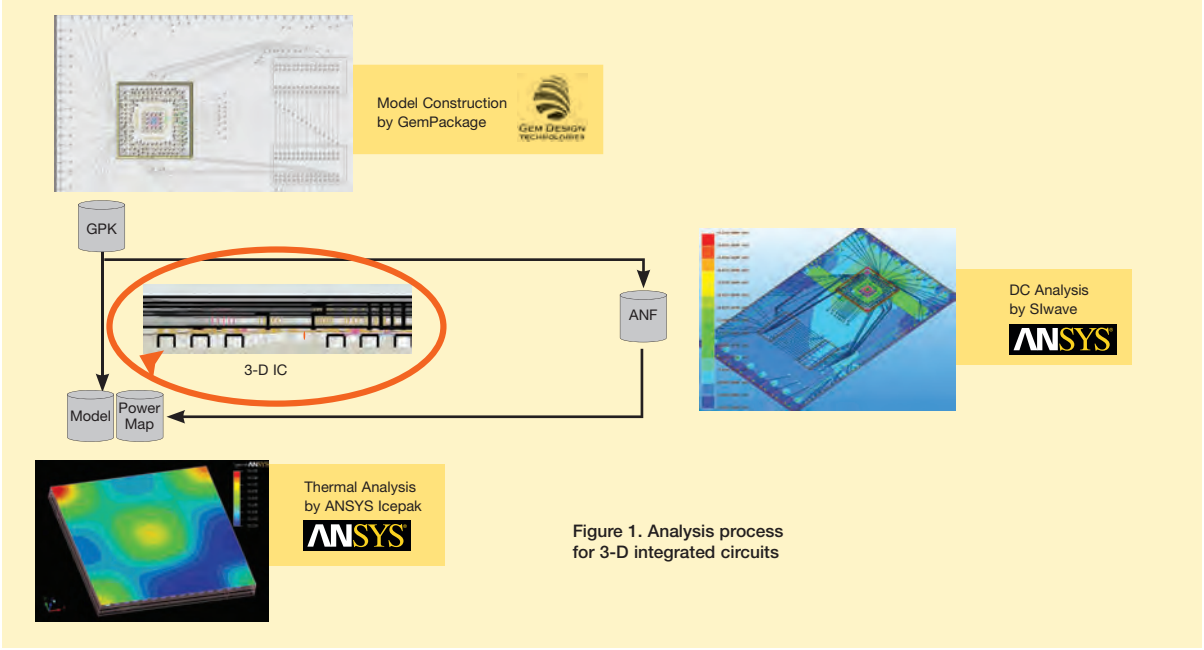

Figure 1. Analysis process for 3-D integrated circuits

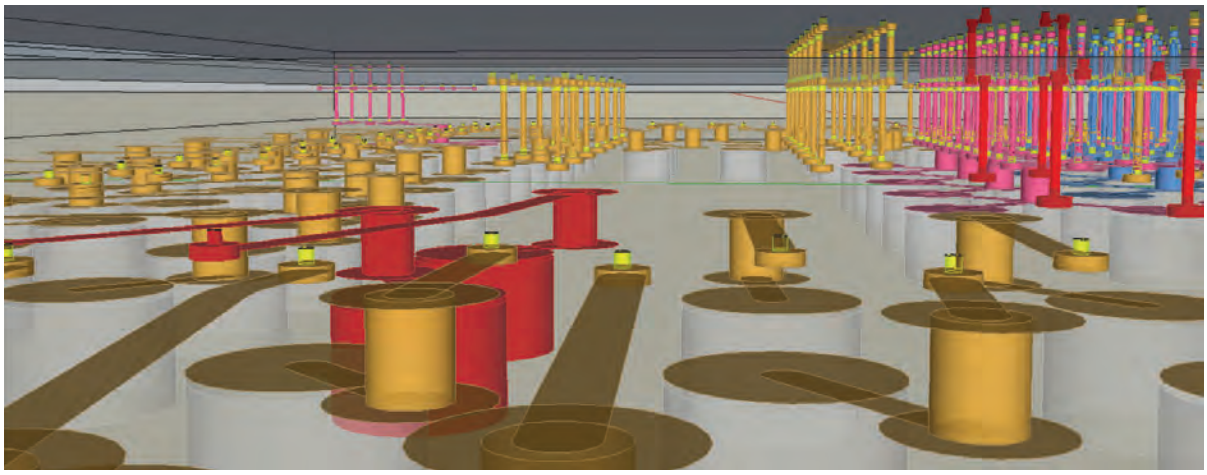

Figure 2. Three-dimensional representation of stacked chips connected by TSVs shown as red columns

single 3-D IC modules with stacked ICs that together perform multiple functions for a complete electronic system. The software supports a wide range of packaging structures from wire bonding to TSVs to complex hierarchical chip and package designs. Before going to detailed design, chip, package or board designers work with GemPackage as a common tool to optimize net assignments in package IOs and chip IOs in the chip–package–board global view.

To demonstrate this approach, models were created for a sample problem involving three chips stacked and connected by TSVs and pattern routings in redistribution layers (RDLs). Die sizes were 10 millimeters square. Die thicknesses were 100 µm each for the top and middle chips and 200 µm for the bottom chip. The top chip had IOs on the bottom surface only. The other two chips had TSVs for through connections and face-down IOs for bottomward connections. All TSVs were treated as 20 µm diameter columns, and IOs (including TSVs) were arranged on a 200 µm pitch grid (Figure 2).

Nets and routings were represented as follows: The main power supply (power/ground net pair) was installed at the center of the chip and connected by stacked TSVs arranged in a seven-by-seven grid. TSVs were also used in connecting zigzag-pattern horizontal routings for signals on the chips. RDLs between the three chips had 20 µm spacing, while those on the bottom of the lowest chip had 60 µm spacing. The bottom RDL contained ball pads on a 600 µm pitch 15-by-15 ball grid array (BGA). To study the effects on electrical and thermal performance, engineers modeled this seven-by-seven grid "standard" floor plan design as an 11-by-11 manytsv model, shown in Figure 3, with more TSVs for the main power source.

For analysis, two Ansoft neutral files (ANF) were created: one for the SiP package and another for board-level design. Files were combined in SIwave to configure the entire system. For a static DC analysis, transistor leakage currents were assumed constant, so chips were modeled as resistors in the power circuits and material constants set accordingly. SIwave software calculated power consumption in RDL power routings and stored the result in a file that is compatible with ANSYS Icepak software (Figure 4).

From the 3-D IC analysis, power consumption in the power routings was calculated as 0.15 Watts (W) for standard design and 0.1 W for the manytsv design. This difference was attributed to the greater number of TSVs, creating more current paths with less equivalent resistance and improved IR drops.

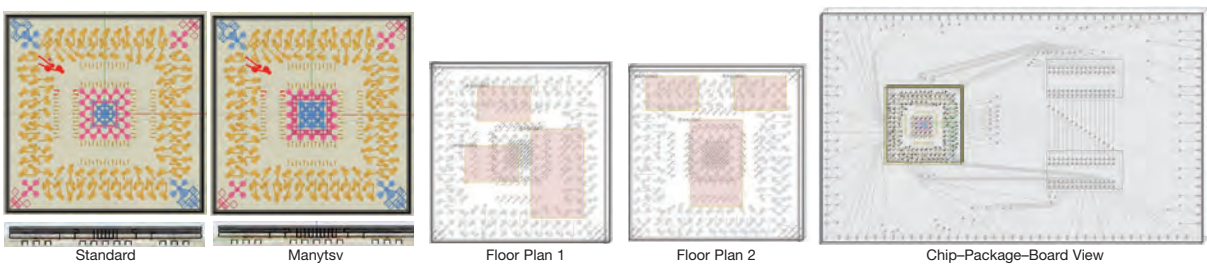

Figure 3. Physical models created by GemPackage

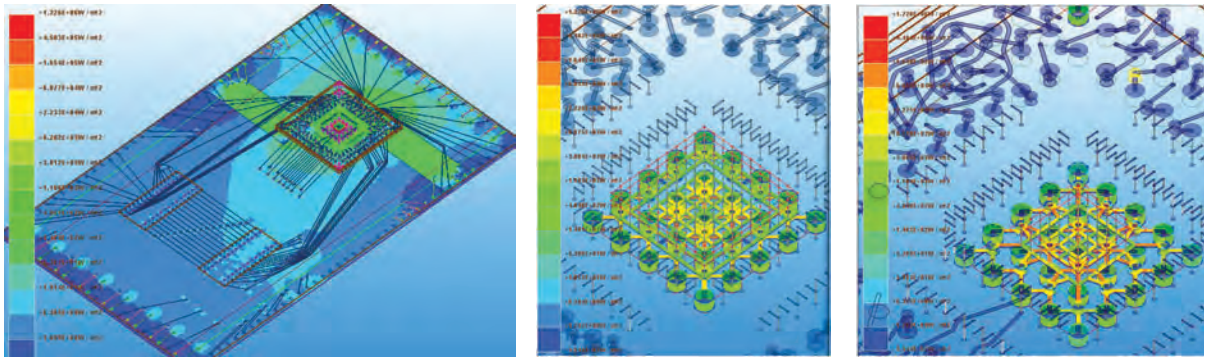

Figure 4. DC SIwave simulation showing power distributions for the entire system (left), seven-by-seven standard (middle) and 11-by-11 manytsv (right) designs

For thermal analysis, GemPackage created a model file that ANSYS Icepak software opened as existing data. To simplify meshing, TSVs were represented as tall rectangular boxes (instead of round columns). To account for effects on thermal conductance, RDL patterns were imported into ANSYS Icepak using the extended Gerber format. ANF can be used in ANSYS Icepak 13.0 to import these RDL patterns. SIwave calculated power consumption in routings, which was imported as distributed heat source cells into ANSYS Icepak.

Top and middle chips were assumed to have 0.1 W planar uniform heat sources, with a value of 0.3 W for the bottom chip. Uniform power relates to the chip. RDL power distribution is computed by SIwave. Boundary conditions were set so that heat flowed out the bottom only. Thermal analysis results indicated that manytsv shows a larger temperature drop at the center of the top chip caused by increased thermal conductivity in the Z-direction as a result of more TSVs and indirectly by more micro-bump balls and RDL patterns. Joule heating in power routings was considered by importing resistive losses from SIwave. This also affected thermal distribution and increased temperatures at the center of the top chip (Figure 5).

To consider different layouts, two versions of floor plans were created for the middle chip. The biggest block was attached with a 0.05 W heat source, and two other small blocks were attached with 0.025 W each. Simulation shows that the bottom chip gets hotter than the upper chip, since heat flows downward. In this way, coupled simulation tools were used to check thermal issues at TSVs in high-density 3-D IC modules.

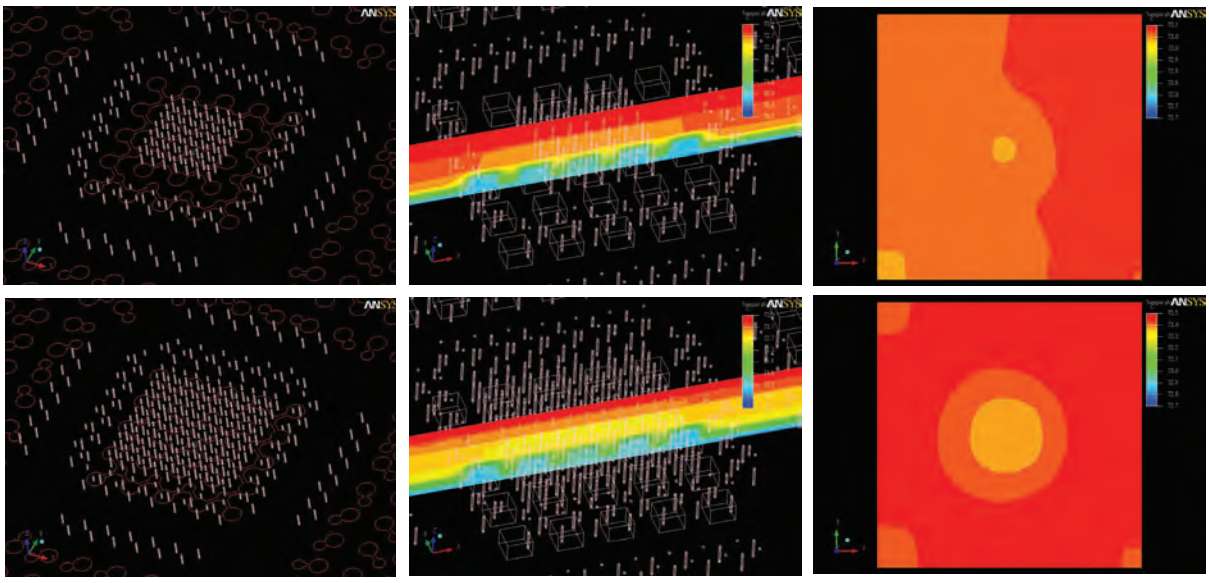

Figure 5. Thermal analysis result obtained using ANSYS Icepak for TSV floor plan layouts (left), power consumption (middle) and thermal distribution (right)