Seeing the Future of **Channel Design**

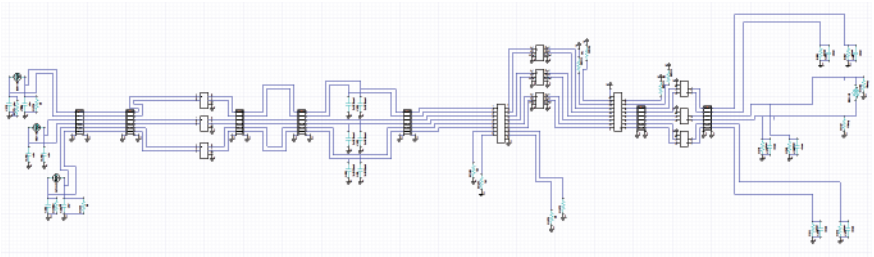
NVIDIA uses VerifEye and QuickEye as an extension to traditional SPICE-level simulation approach to design high-performance graphics solutions.

By Chris Herrick, Technical Lead, Ansoft LLC

It's hard to imagine, but there was once a day when slick high-resolution graphics were not the norm. With increasing monitor sizes as well as ever-sharper digital media and spectacular gaming technology, computer graphics have progressed in an amazing way. NVIDIA® is a world leader in visual computing technologies and the inventor of the GPU, a high-performance processor that generates breathtaking, interactive graphics on workstations, personal computers, game consoles and mobile devices. NVIDIA serves the entertainment and consumer market with its GeForce® graphics products, the professional design and visualization market with its Quadro® graphics products, and the high-performance computing market with its Tesla™ computing solutions products.

One of the hardest challenges when designing these high-performance graphics solutions is ensuring that the communication link is clear between the pixel generation and pixel display. That means the signal, representing a zero or one, originating at one part of the system needs to propagate undistorted to another area so it may be detected without errors.

As data link speeds increase, so do the problems that affect signal quality. Every part of the physical routing channel has some influence on the propagating electromagnetic fields and, thus, on the detected waveform. The channel could be assembled from many combinations of elements including packages, transmission lines, cables, connectors and vias. A discontinuity or impedance



Full channel simulation using the Ansoft Designer tool

mismatch to the propagating signal could occur at any point along the transmission path.

A common tool for the signal integrity engineer is circuit simulation. By modeling the channel virtually, engineers are able to predict waveforms not only at the receiver but for each section of their modeled channel. This level of detail allows engineers to verify signal detection as well as to determine the contribution of signal distortion for each section of the channel. To improve or optimize a system, the sections of channel that produce the greatest signal distortion can be identified, and intelligent changes can be made. These changes could include geometric variations, elimination or addition of components, or material selection.

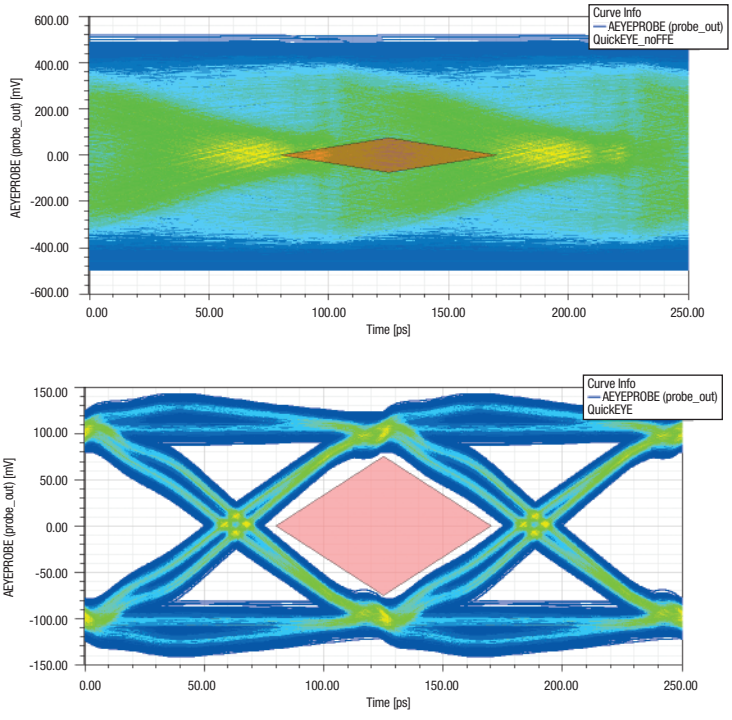
In order to construct the virtual channel, NVIDIA chose the Ansoft Designer tool as its simulation environment. Ansoft Designer allows the engineer to assemble each piece of the channel as a black box model. These models may comprise measured data, simple circuits, SPICE components or dynamic links into any of Ansoft's circuit extraction tools. These individual models may be rearranged, bypassed or parametrically varied, providing the engineer with the ability to test all possible configurations. This high-level schematic approach also allows the design to be easily shared among different groups, which then can quickly see what is being modeled and provide input into the design.

Under the hood of Ansoft Designer software lies the powerful circuit simulator product Nexxim. Nexxim technology is a high-capacity, high-accuracy engine for linear network analysis, transient analysis, harmonic balance, fast convolution and statistical methods. With this array of different simulators, NVIDIA is able to look at channel performance from many different perspectives, all from within the same environment.

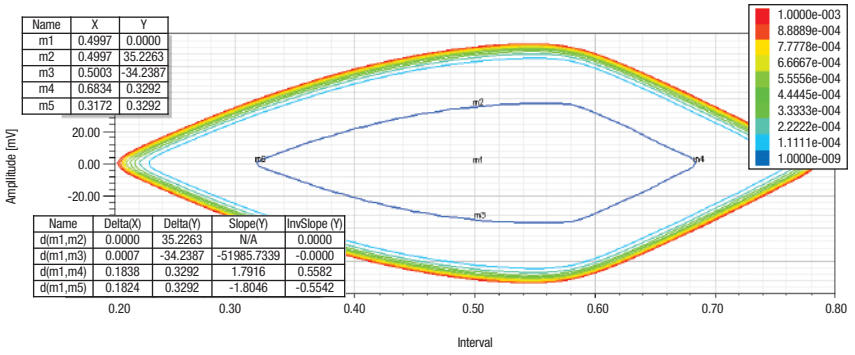
The traditional signal integrity simulation methodology is to perform a transient simulation. Using this approach, the driver is toggled for a length of time and the voltage is monitored at receiver. A common way of viewing this received data is to overlay the voltage versus time for each bit period, or unit interval. The resulting graph is called an eye diagram, and it can very clearly show whether the received data is able to be detected error free.

Transient analysis is the most accurate means of determining signal waveforms, but it is limited by the scope of the problem. To fully analyze all the variations in a channel with nonlinear devices can take days to weeks. Trying to achieve low bit error rates (BERs) poses an additional challenge. Using transient analysis, simulating enough bits to satisfy a BER of 10^{-12} could take years. In order to satisfy these engineering challenges, Nexxim technology has incorporated two specialized solvers, namely QuickEye and VerifEye.

According to Ting Ku, director of signal integrity at NVIDIA, "The obvious reason for statistical transition is related to simulation coverage. Given there is a finite amount of time and machine resources, the statistical approach gives engineers systematic coverage without



The top image demonstrates the receiver eye on a channel where the data cannot be recovered; the bottom is a clean eye diagram where the data is recoverable.

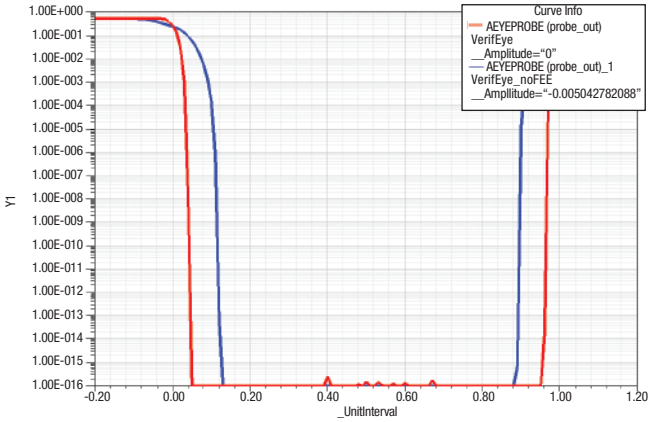


Eye contour plot generated with the VerifEye tool

running an astronomical number of simulation corners. One other good benefit of the statistical approach is in dealing with design corner definition by projecting what the final production yield would be. Using the statistical methodology allows engineers to make judgment calls between cost and production yield."

While both QuickEye and VerifEye methods offer significant speedup over transient analysis, each offers a different solution to the problem at hand. QuickEye is a fast convolution-based method that allows the user to explicitly define a bit pattern that is sent and to view the resultant waveforms. VerifEye is a purely statistical-based approach that characterizes BER of a channel down to 10^{-16}.

Both of these methods begin analysis the same way by first computing the transfer function of the channel. This computed channel response is assumed to be linear–time invariant. For QuickEye, the channel response is then convolved with a user-specified bit sequence to obtain a time vs. voltage waveform. For VerifEye, a cumulative distribution function is derived from the step response based on the conditional probability of various bit transitions. The main outputs from these analyses would be an eye diagram from QuickEye and a bathtub or a statistical eye contour plot from VerifEye.



Bathtub curve of feed forward equalization performance generated with the VerifEye tool

While it is critical to fully characterize the entire passive channel, the scope of the analysis does not stop there. In order to compensate for frequency-dependent effects of the channel, such as inter-symbol interference (ISI), NVIDIA uses silicon-based compensation. Additionally, there may be other influences on the signal in the form of jitter that must be accounted for. This jitter may be seen at both the driver and the receiver.

As part of its investigation into silicon-based channel compensation, NVIDIA can use either QuickEye or VerifEye to evaluate feed forward equalization (FFE) or decision feedback equalization. If the silicon has already been characterized, the number of equalization taps and their respective weights can be added to either the driver or receiver on the channel. During early stages of design, the Nexxim tool can be used to automatically calculate the ideal weights necessary to invert the effects of the channel on a bit stream.

Jitter characterization, and its inclusion in simulation, is another area critical to NVIDIA. Without including all sources of noise, accurate BER simulations would be impossible. Random jitter (RJ) and duty cycle distortion (DCD) can also be added to each driver. ANSYS also learned from this partnership with NVIDIA that the inclusion of periodic jitter (PJ) and sinusoidal jitter (SJ) would be useful features so ANSYS has since enhanced the Nexxim tool to include this capability. Deterministic jitter (DJ), based on ISI, will inherently be modeled by the channel's transfer function. At the receiver, the source jitter will accumulate with the DJ of the channel to create a new jitter distribution. This jitter in combination with the jitter defined at the receiver, either RJ or a user-defined distribution, will account for the total jitter (TJ) of the channel. Reducing TJ is the main objective when designing a channel for low BER.

With ever-increasing bit rates and channel complexity, the landscape of signal integrity analysis is changing drastically. Transient analysis can no longer be relied on as the sole means of channel simulation, especially when trying to achieve extremely low BER. This challenge has been met head on at NVIDIA by adopting QuickEye and VerifEye analysis into their design process. ■