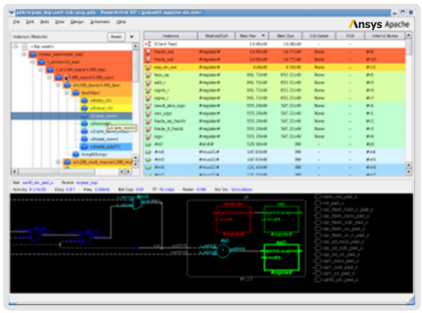
APPLICATION BRIEF

Ansys PowerArtist
Industry-leading Comprehensive RTL Design-for- Power Platform: Analyze, Debug, Reduce

Ansys PowerArtist is the register-transfer level (RTL) design-for-power platform of choice for semiconductor design. From handheld to wall-powered chips ranging from mobile, processing, networking, automotive and IoT applications, PowerArtist is used to analyze and reduce power early in the RTL development cycle for the highest impact.

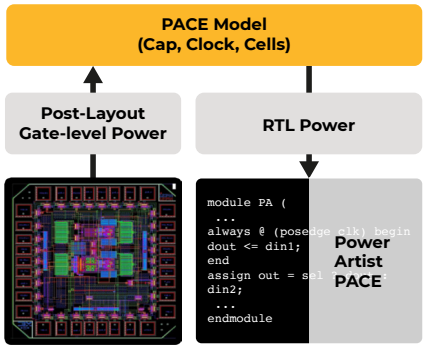
Physically-Aware RTL Power Budgeting

Compared to traditional gate-level methodologies, PowerArtist provides rapid turnaround on multimillion instance designs for fast what-if RTL analysis. But, the more advanced the process node, the greater the influence physical design considerations have on power. Pioneering PACE (PowerArtist Calibration and Estimation) technology models physical effects such as clock tree and mesh, wire capacitance, and glitch, to deliver consistent RTL power accuracy, enabling reliable design decisions.



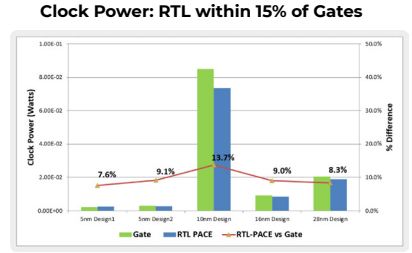
Comprehensive Power Analysis and Exploration

Early visibility to power and power bugs plays a vital role in meeting time-to-market and first silicon success goals. PowerArtist comprehensive set of features enable activity, average, and peak power analyses with multiple views across design categories, power, and clock domains. Based on an RTL functional abstraction of the design, the best-in-class interactive graphical power debug platform and TCL-based interface for customized queries enable you to quickly identify and debug power hotspots.



Analysis-Driven Automated Power Reduction

Power effciency is a critical requirement across applications. PowerArtist identifies all wasted toggles within the design. High-impact techniques identify hierarchical clock and data gating opportunities. Automated combinational and sequential techniques identify new clock enables, redundant memory accesses, and redundant activity in cones of logic with a high-performance architecture not limited to sequential stages. Reductions are based on production-proven physically-aware analysis to ensure that identified RTL changes are predictable and minimize design impact.



Early Power Profiling of System Activity

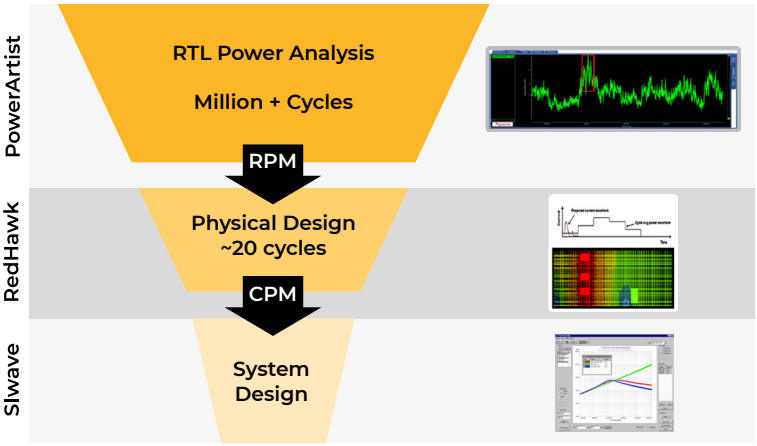
Traditional power methodologies are based on design activity simulated for a few microseconds, putting the design at risk from power issues that can be exposed by real-life world stimuli. PowerArtist provides industry's fastest power profiling, enabling per-cycle analysis of hundreds of milliseconds of activity, such as OS boot-up, within hours – orders of magnitude faster than standard approaches. PowerArtist's dynamic activity streaming and critical signal interfaces with emulators cut the time to power by an order of magnitude.

Regressions Based on Power Efficiency Metrics

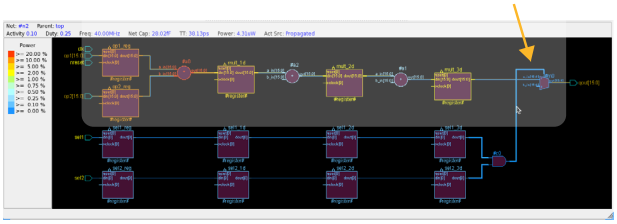
Regular and rigorous monitoring of power and power effciency metrics throughout the design development cycle avoid costly, late surprises by isolating power issues when they happen. PowerArtist provides a complete regression framework with defined power effciency metrics, data mining interface, and regression utilities that compare and plot metrics across design versions to prevent power creep.

RTL-Driven Power Grid Integrity

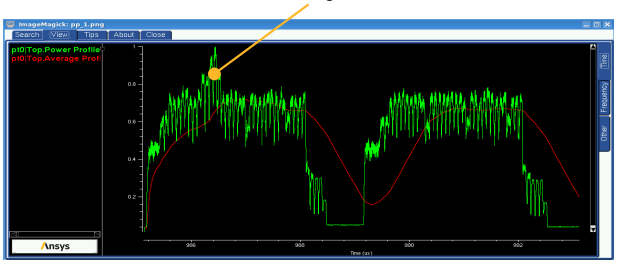
The power delivery network (PDN) across the chip, package and system must deliver power across all complex modes of operation. Reduced noise margins at advanced process nodes further challenge the PDN, and it must account for critical scenarios including peak power and di/dt early in the design process. Rapidly isolating a power-critical subset from millions of RTL cycles of activity, PowerArtist generates a unique RTL Power Model that interfaces with Ansys RedHawk to deliver a seamless solution for early power delivery network prototyping and increased sign off coverage.



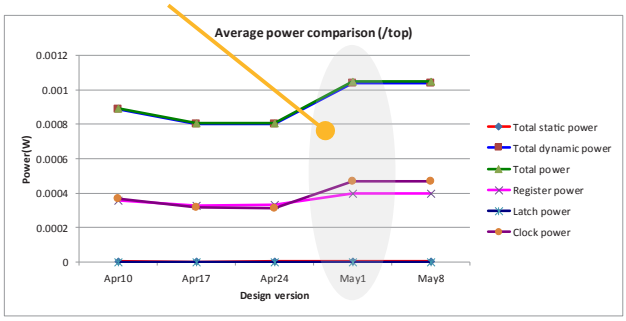
Observability-based clock gating when sel is 0



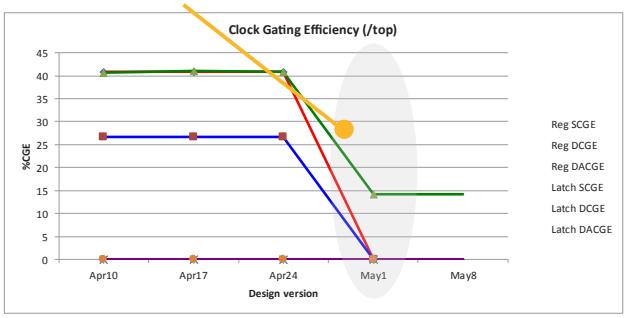
1000X Faster Per-cycle Power Profile



Increase in power



Drop in CG Efficiency



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