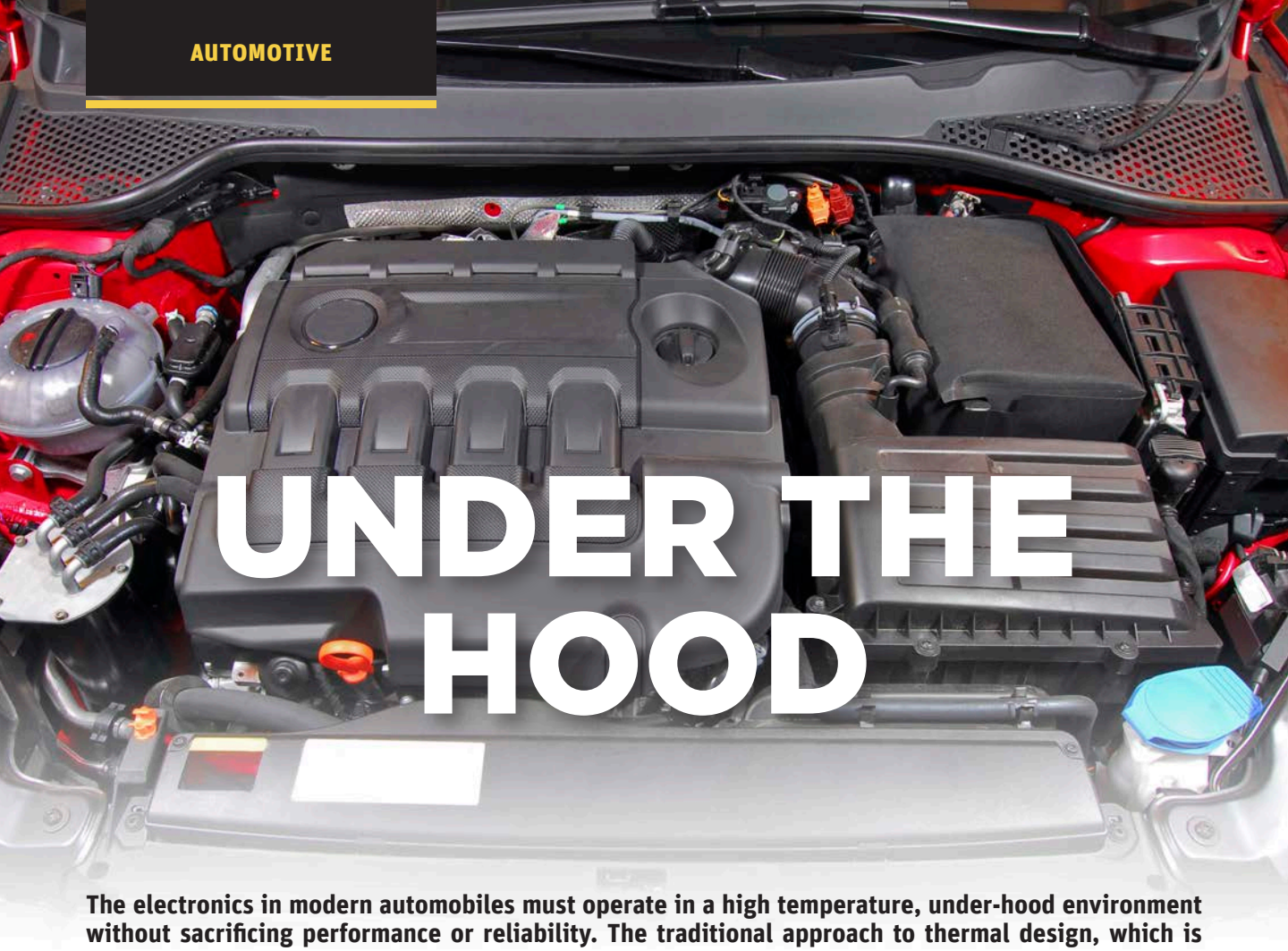


UNDER THE HOOD

The electronics in modern automobiles must operate in a high temperature, under-hood environment without sacrificing performance or reliability. The traditional approach to thermal design, which is based on the assumption that the entire integrated circuit (IC) is at a constant temperature, is fast becoming obsolete as higher power dissipation and shrinking form factors make thermal design more critical. NXP engineers use ANSYS tools to calculate temperature and current density throughout the device, making it possible to predict local junction temperatures more accurately and perform thermal-aware electromigration (EM) analysis.

By Jehoda Refaeli, NXP Semiconductors, Austin, USA

The automotive environment presents one of the most difficult thermal challenges for electronic component designers because ambient temperatures in under-hood applications can reach 135 C. The thermal challenge is increased because the electronic components are exposed to water and dust, so enclosures must be sealed against the elements and, in most cases, cannot use a cooling fan due to reliability concerns. The design team is faced with the challenge of ensuring that device junction temperatures remain at safe levels — typically under 150 C — while also guarding against failure due to EM (the mass transport of a metal due to the momentum transfer between conducting electrons and diffusing metal atoms). Over time, the mass transport in the lattice of interconnect material leads to connection failure and circuit malfunction. Applications in which high direct current densities are used, such as integrated circuits, are especially impacted by EM. As the size of ICs decreases, the practical impact of EM increases. Automotive ICs are particularly susceptible to EM because this phenomenon increases as a function of temperature, and the hot under-hood environment combined with the increasing heat flux of modern electronics drives up chip temperatures.

Traditionally, NXP engineers used design rules to check and correct EM problems. This approach assumes a uniform worst-case temperature across the chip, when actually temperatures vary widely between hot spots and cooler areas. As

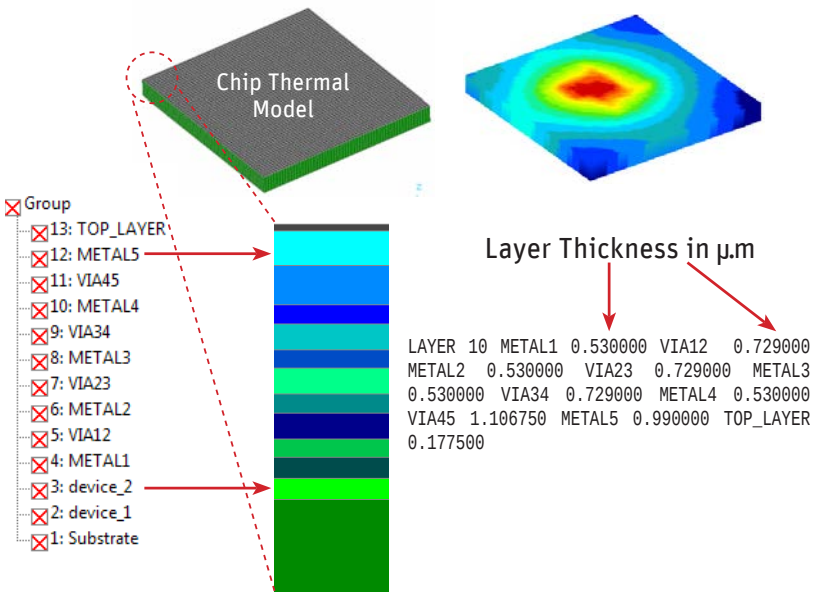
The automotive environment presents one of the most difficult thermal challenges for electronic component designers.

NXP increased the speed and power of its devices, the company found it progressively difficult to meet EM specifications due to the large margin of error that the traditional approach produced. With ANSYS RedHawk, ANSYS Totem and ANSYS Sentinel-TI, NXP engineers can, for the first time, accurately determine the junction temperature of individual complementary metal oxide semiconductor (CMOS) devices and calculate EM based on actual temperatures. The ability to make design decisions based on thermal gradients enables NXP to increase product performance while ensuring reliability and reducing time to market.

AUTOMOTIVE ELECTRONICS THERMAL CHALLENGES

An NXP automotive device, consisting of a memory chip stacked on top of a system-on-chip (SoC) and connected via Cu pillar technology, is used for powertrain, safety, motor and battery control. This type of 3-D IC stacked device can reduce power consumption and improve communication speeds, but the complex thermal interaction between chips is impossible to analyze using conventional methods. For example, the stacked component needs to be validated with high power on the bottom and low power on top when a logic operation is performed, and with low power on the bottom and high power on top during memory read/write situations. Each device must also be validated with manufacturing variation taken into account. The two possible conditions that need to be evaluated from a thermal standpoint are slow processing/low leakage and fast processing/high leakage.

▲ Typical NXP automotive component consists of a memory chip stacked on top of a system-on-chip (SoC).



▲ Each layer of chip is divided into elements with dimensions in microns to create a chip thermal model (CTM). The chip thermal model contains a multi-layer structure of thin layers on top of a silicon chip and the temperature profile with model resolution in microns.

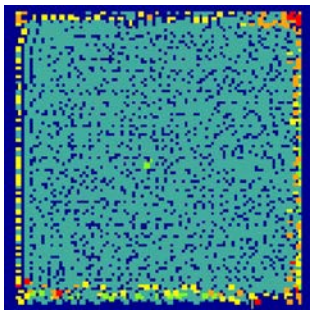
In the past, thermal design was normally carried out using systems-level thermal analysis, which predicts complete system temperature based on sources of heat and thermal transfer to the environment. But this approach is limited because it does not take the detailed design of the chip into account. In a major simplification, power is usually considered to be dissipated uniformly across the chip, and the simulation predicts a uniform temperature for the entire chip. This temperature is then used as the estimated junction temperature for every CMOS device on the chip. The uniform temperature is also used in the electronic computer aided design (ECAD) system as the basis for design rule checks (DRCs) for EM signoff. The inherent assumption of uniform temperature in this approach leads to unreliable results. Previously, this limitation was addressed by using a large margin of safety to account for temperature gradients. But today, the increase in heat caused by putting more CMOS devices in a smaller volume makes it difficult or impossible to meet thermal signoff requirements using traditional methods.

CALCULATING TEMPERATURE PROFILE THROUGHOUT THE CHIP

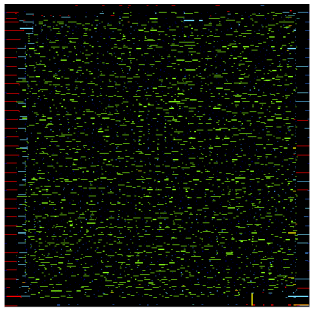
NXP addresses this challenge using the ANSYS semiconductor thermal toolset to model chip details and determine the power density and thermal gradients at any point. Modeling every wire and device in detail would be too compute-intensive, so chip design is simplified by dividing each layer into rectangular elements. Each element contains information about the power and metal layer

The design team is faced with the challenge of ensuring that junction temperatures of devices will remain at safe levels while also guarding against failure due to EM.

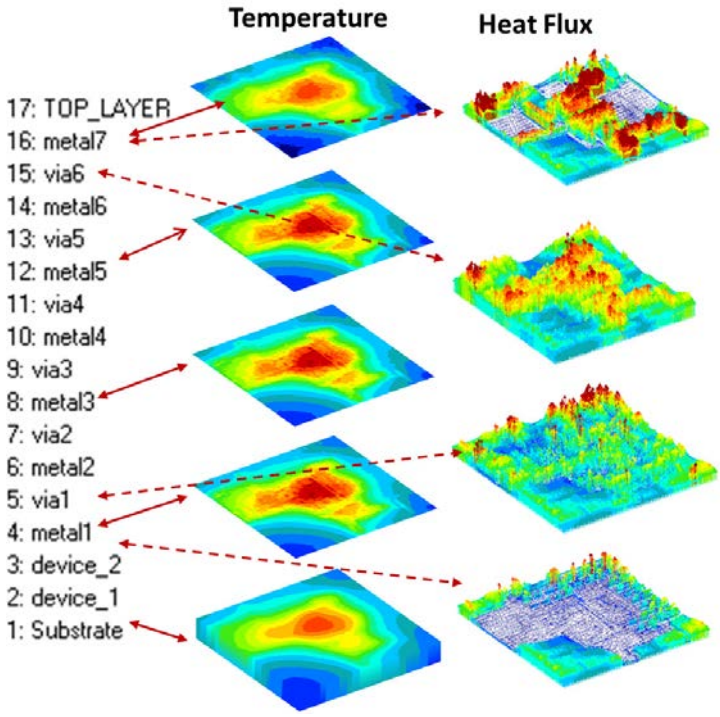
M2 Temperature Map



Signal EM (M2) Map



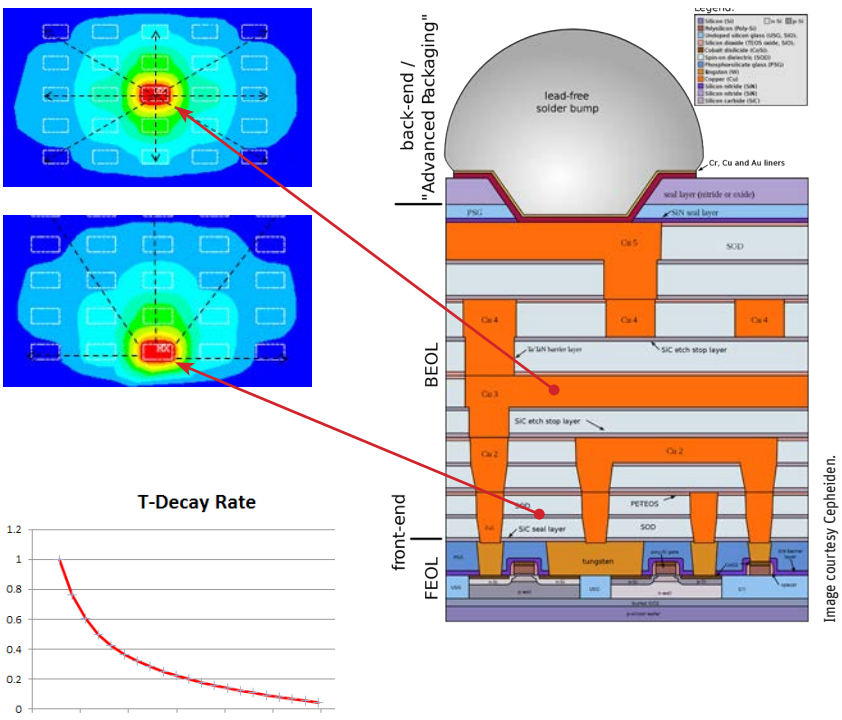
▲ Temperature and EM maps



▲ CTM is used to provide tile-based temperature-dependent power density and per-layer metal density maps.

density based on the detailed design, as well as the thermal conductivity between layers. This information is used by ANSYS RedHawk (for SoCs) and by ANSYS Totem (for custom digital devices such as memory dies, as well as analog and mixed-signal ICs) to calculate the temperature profile across the chip. This becomes the base temperature profile of the chip. The temperature gradients on the chip are dominated by the power distribution of the chip's CMOS devices.

Wire temperatures on a chip are further increased by Joule heating and vertical thermal coupling from devices to wires. In the past, Joule heating was not a major concern, but today, with wires placed closer to each other than ever before and buried in low-thermal-conductive dielectric materials, Joule heating of wires can no longer be ignored; therefore, a Joule heat model of each wire is created using the root-mean-square (RMS) current on a signal wire, or the average current on a power or ground wire, along with thermal coupling. The temperature change of each wire is calculated directly based on the power, size, aspect ratio, elevation, thermal conductivity and thickness of dielectric



▲ Joule heat is calculated for each wire and its neighbors.

NXP addresses this challenge using the ANSYS semiconductor thermal toolset to model the detail of the chip and determine the power density and thermal gradients at any point.

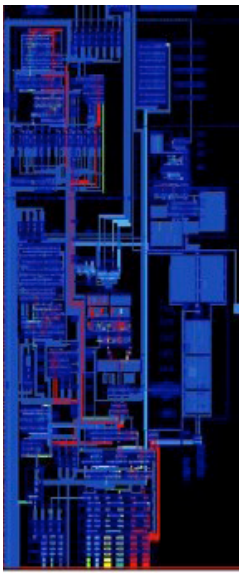
material using a simple linear superposition principle, so minimal computational effort is involved. The localized thermal effects of Joule heating on current density and temperature are added back to the thermal analysis based on the chip thermal model (CTM).

Dynamic power, which relates to the operation of devices on a chip, was dominant in traditional designs. However, the proportion of static power, driven by leakage current, is catching up in new chip designs. Static power scales with temperature, so this phenomenon is particularly important in under-hood automotive designs. The power map for distributed temperature on the chip is used to calculate static power. The static power generates additional self-heating, and the CTM and EM analyses are updated to take this into account.

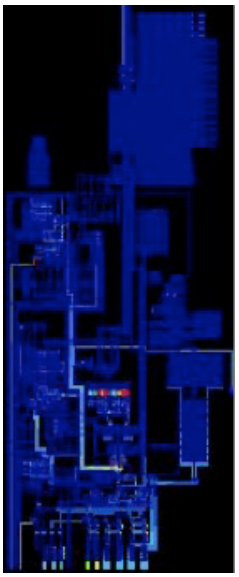
ANALYZING THE CHIP-PACKAGE-SYSTEM

The CTM model for each chip along with 3-D IC and package details is passed to ANSYS Sentinel-TI, which performs a CTM-based thermal analysis to generate converged temperature and power maps of the complete system. The system thermal boundary conditions are fed back to RedHawk and Totem for use in re-running the CTM-based thermal analysis to take the effects of the other chip and the package into account. The converged power map produced by Sentinel-TI can also be passed to ANSYS Icepak, which can perform a complete system analysis and simulation of the complex airflows around the package.

Rather than relying on a single temperature value representing a whole chip, NXP engineers can now view plots that show the temperature at any point in the chip so they can easily identify individual devices with excessive junction temperatures. They can also perform thermal-aware EM checks based on the actual temperature experienced by each wire on the chip. Based on this information, engineers can make corrections into the design early in the process to eliminate troublesome hot spots. They can also address different operating and process conditions, which were not considered in the past, simply by re-running the model based on the relevant conditions. The result is that NXP engineers can improve the performance and reliability of critical automotive semiconductors while reducing time to market.

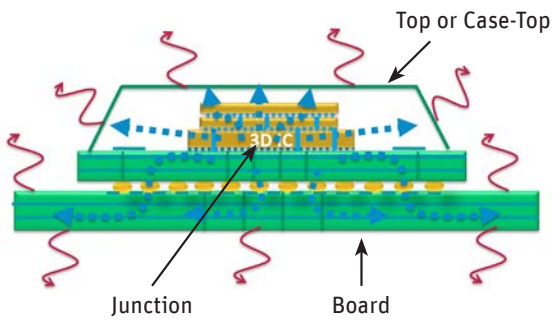


Wire Temperature Map



Wire EM Map

▲ Actual wire temperatures are used to calculate thermal-aware electromigration (EM).



▲ ANSYS Sentinel-TI analyzes the complete thermal flow path of the ICs, package and system. 3-D IC and package details are crucial in accurate on-chip thermal analysis.

The ability to make design decisions based on thermal gradients enables NXP to ensure reliability and reduce time to market.