AN APPLICATION BRIEF FROM ANSYS, INC.

High-Speed Serial I/O Design Using Response Surface Modeling

ABSTRACT

Response surface modeling (RSM) enables engineers to consider all aspects of a design while only modeling a fraction of all unique possible design variations. Today's high-speed digital channels, such as PCI Express® (PCIe), encompass so many design variables that solving for every unique combination is not feasible. Response surface modeling provides a statistically based solution to this problem. This application brief shows how a statistical fit is made to model the outputs of a particular design as a function of changes to input variables. The example architecture chosen is PCI Express 3.0. The scenario is this: An engineer is tasked with providing reference designs during the pre-layout design stage. A design of experiment (DoE) table is created and used to select solution points. Response surfaces are then generated to represent eye width and height for all possible design configurations. The next step is to examine sensitivity plots. This allows the engineer to establish which design variables are statistically insignificant and may be fixed. Narrowing the number of variables and rerunning a smaller DoE often leads to more-accurate response surfaces. An optimization algorithm of worst-case scenarios are considered to identify if and what design configurations lead to eye height and/or width violations. Lastly, the PCIe specification rules are applied to worst-case designs to check for pass/fail criteria. This information then helps to establish if all design combinations are sufficient to meet the PCIe standard. If failures occur, an associated defects-per-million rate is determined.

PRODUCTS USED

DesignerSI™, ANSYS® DesignXplorer™

KEYWORDS

High-speed channel design, design of experiments, DoE, response surface modeling, defects per million

PROBLEM DESCRIPTION

In a high-speed digital channel such as PCI Express, there are many design factors, all of which can affect signal quality. In this application brief, a PCI Express 3.0 channel is described and analyzed. The PCIe channel architecture consists of a package, socket, PCB, connector, PCIe card and package. For this example, three differential pairs are simulated. The variables for each channel are package trace length, 12 package models, six PCB via configurations, PCB trace length, PCB trace impedance, card trace length, card trace impedance, PCIe card trace length and transmit/receive (TX/RX) characteristic impedances.

Many other factors could have been included, such as copper roughness in traces, different breakout architectures, etc. In statistical terms, these variables are called factors. If each factor has a few different variations or levels, it's easy to see how the problem set becomes extremely large. In fact, it scales as follows:

$$\text{Number of unique permutations} = \text{Levels}^{\text{Factors}}$$

To analyze the above problem for a large number of design variations, DesignerSI technology is linked with ANSYS DesignXplorer software. This linkage allows DesignerSI to simulate the various channel topologies that are determined by ANSYS DesignXplorer.

If there are 25 factors or variables and there are only five different variations or levels to each, then there are 5 to the 25th power of unique combinations to consider. That number is so large that it is impractical to consider solving all combinations directly. However it is easy, and very practical, to utilize response surfaces to address this issue. Response surfaces are simply an extrapolation of data points representing a smaller subset of the entire solution space. The determination of which solution points to solve is decided statistically through a method called design of experiments (DoE). In this example, ANSYS DesignXplorer to creates the response surface using the DoE approach. Since the focus is on showing the methodology from a system level, there is no deep detail provided here on generation of the DoE table points..

The response surfaces are created from the solved DoE table, allowing examination of the output variable values. For this example, eye height and eye width have been defined as the output variables. The response surfaces allow the user to determine the dependency of eye height and width as a function of the input variables. Additionally, it allows determination of worst- and best-case design configurations. However, this determination can be cumbersome and, as a result, it is often useful to utilize an optimization algorithm (discussed later in this brief). Because the created response surfaces allow examination of the sensitivities of each input and output variable, it is possible to reduce the number of input variables when a variable is found to be statistically insignificant on the output. The variables that show minimal statistical significance are set as a chosen constant in the design. This means that there are fewer variables in the design. A new smaller DoE table is then created and run. While this is not always necessary, initially large variable sets minimizing the number of variables can lead to more-accurate response models or quality of model fit.

Quality of model fit is formally referred to as coefficient of multiple determination, or R^2. An R^2 of 1 means a perfect fit, where a fraction such as 0.95 denotes a lesser quality of fit. The commonly accepted engineering standard in this type of design is 0.95 or better.

This example identifyies where the design may fail. Failures specifically relate to when the design fails to meet the PCIe gen 3 eye height and/or width specification. To identify these worst-case situations, this example relies on the ANSYS DesignXplorer direct optimization tool. The optimization algorithm returns candidates that are worst-case scenarios. The example searched for minimum eye width and minimum eye height. If situations occur in which failures are eminent and changes cannot be made to avoid these cliffs, a metric of failure, such as defects per million (dpm), can be provided. The acceptable target for this application is usually 1,000 dpm or lower. It is clear that this type of information is critically important to engineers because they can make recommendations about manufacturability of a design, how a design will perform versus changes in materials or tolerances, and what changes will make or break a successful design.

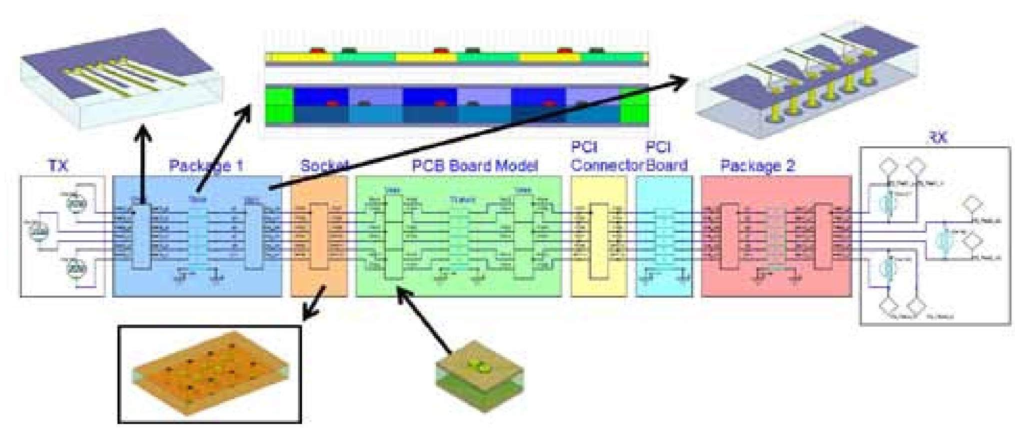


Figure 1. PCIe generation 3 channel in DesignerSI

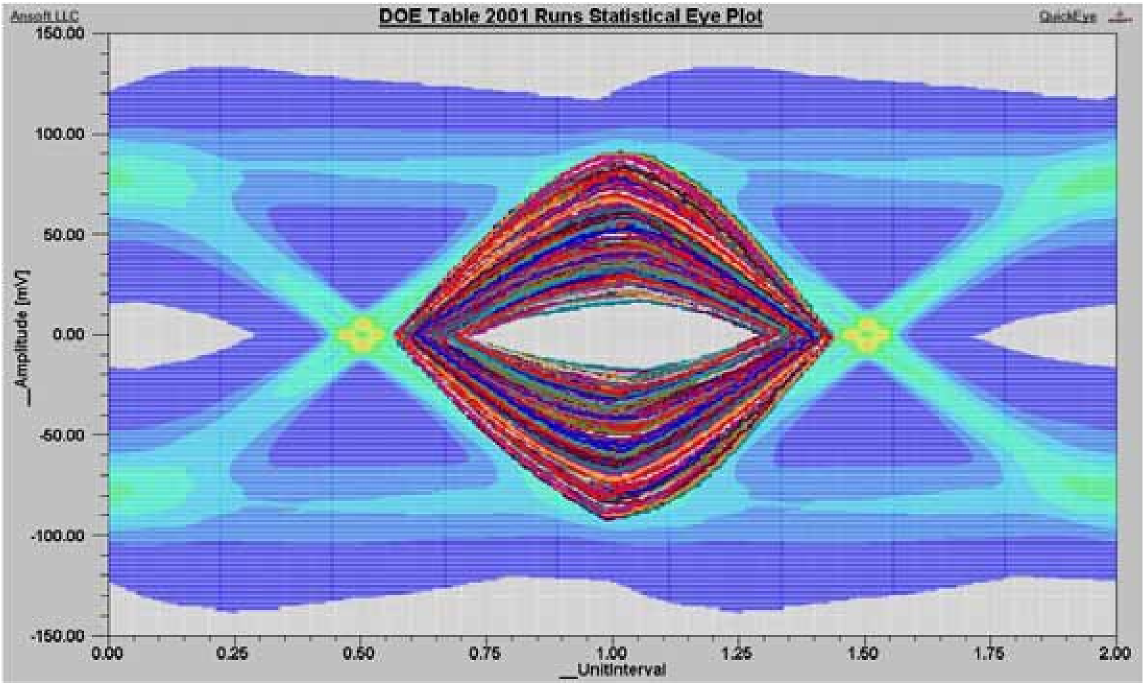


Figure 2. Eye diagrams of all simulations run from DoE table

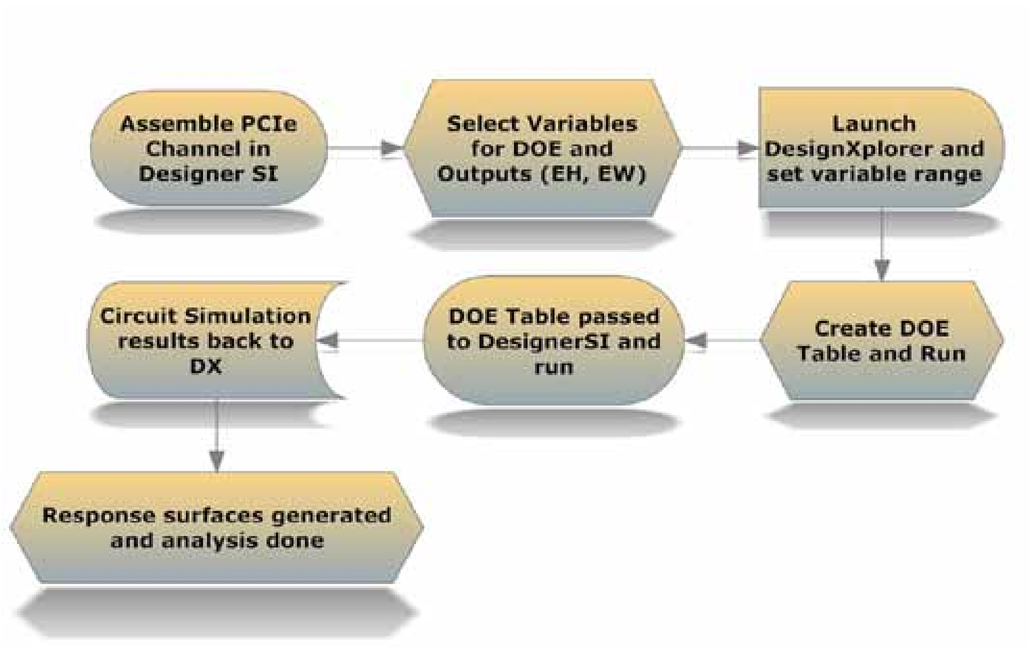


Figure 3. DoE/RSM workflow in DesignerSI and ANSYS DesignXplorer

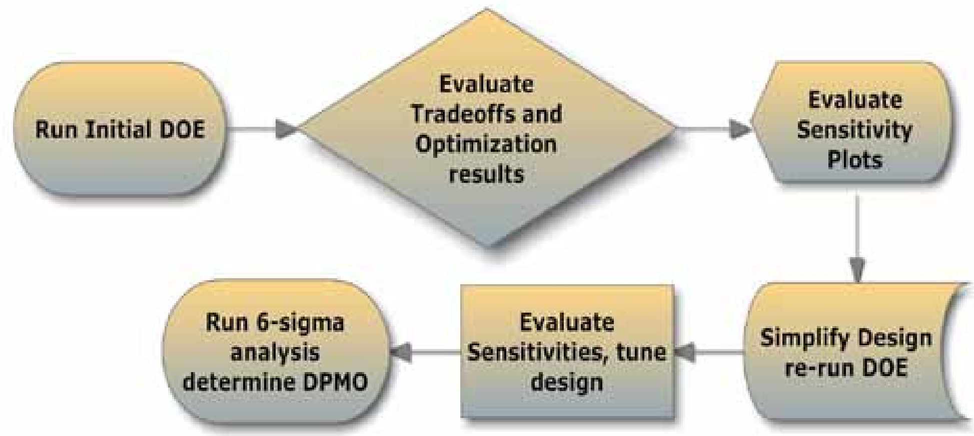


Figure 4: DoE/RSM methodology applied to HSIO channel design for identifying design references

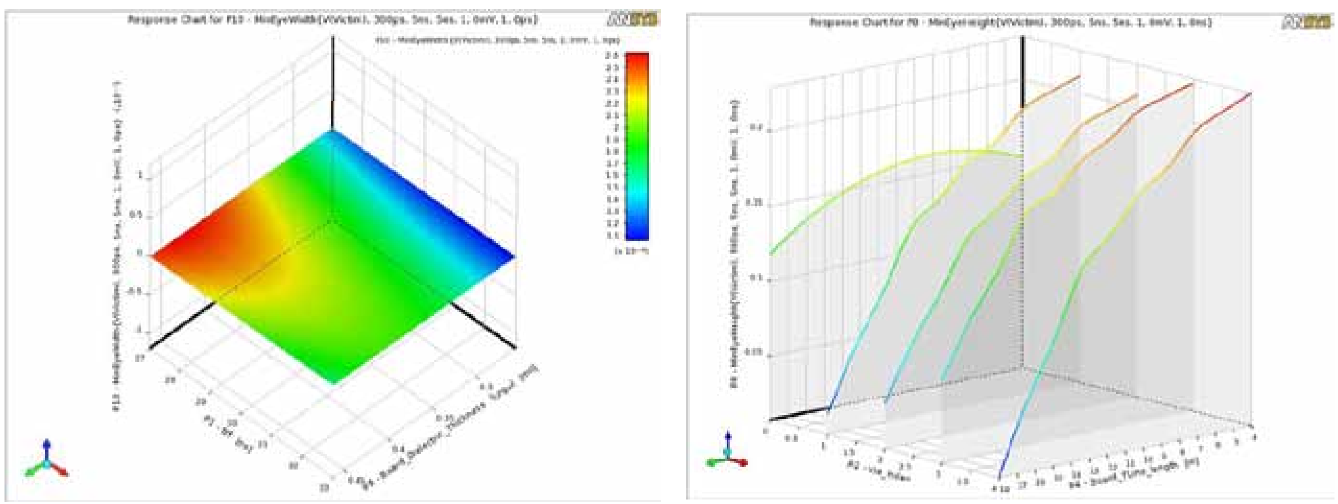
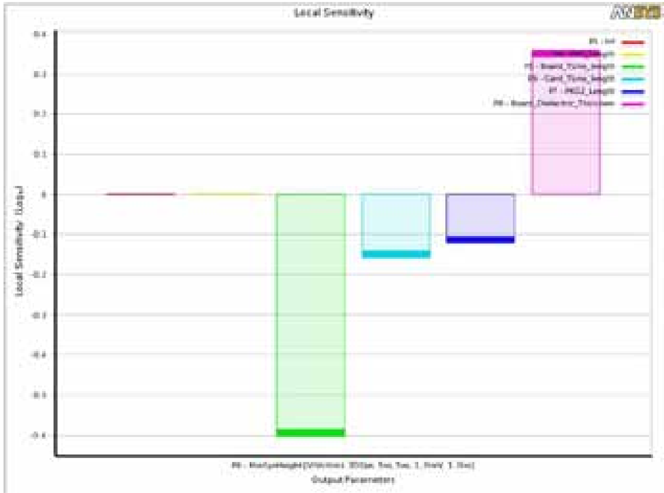


Figure 5. Response surfaces: two continuous input variables and eyes width (left); continuous and discrete input variables and eye height (right)



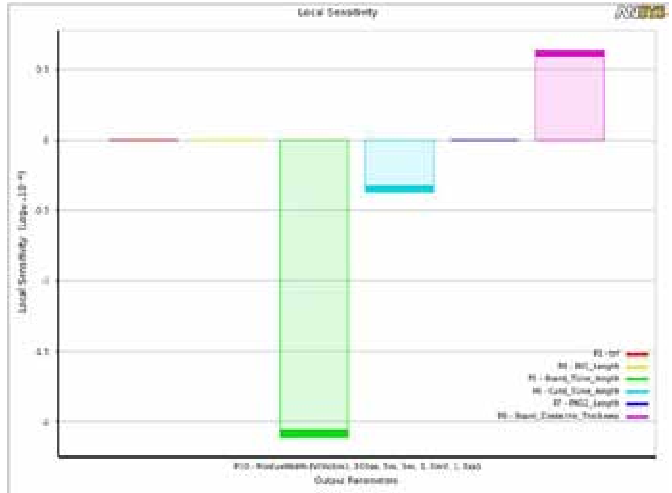


Figure 6. Sensitivity plots: Greater positive number means greater impact on output positively, more neagative means greater negative impact on output.

Candidate Points					
Candidate A	9	4	11.944	1.8677	★★★
Candidate B	8	1	11.688	1.8333	★★
Candidate C	9	0	10.152	1.8075	★★

Figure 7: Optimization results for smallest eye height and width

CLOSING SUMMARY

Response surface modeling enables designers to model and consider all aspects of a complex high-speed channel design. Optimized conditions and worst-case scenarios are obtainable within the set of all possible design combinations within a realistic simulation timeframe. This enables potential design failure achitectures to be identified and understood before the costly manufacturing and test stages.

Using a cohesive tool set such as DesignerSI and ANSYS DesignXplorer improves simulation time and reduces operator error. Transient, statistical transient, peak distortion analysis and equalization schemes are all inclusive within the DesignerSI environment and can be part of the DoE that “improves goodness of fit R^2.”

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