Totem™ Technologies for Analog / Memory / Mixed-Signal Designs

Design Automation Conference 2014
Analog Mixed-Signal Trends & Challenges

- Analog IC market expected to grow to $60B by 2015
- Transition from discrete analog to analog subsystems
- Complex verification and integration challenges

Key Market Drivers
- Mobile Computing
- Automotive Electronics
- IoT/Connected Devices

Technology Trends
- Technology Scaling
- High Analog + Digital Integration
- Increasing Sensor/IP usage

Challenges
- Capacity
- Tighter Reliability Margins
- Concurrent Analog + Digital Analysis
- Sensor/IP Validation and Modeling

$60B Mobile Computing
Automotive Electronics
IoT/Connected Devices

Graph showing Analog IC Revenue growth from 2013 to 2015
Totem: ‘Power-Noise-Reliability’ Platform

- SRAM
- Flash
- DRAM
- IO (DDR, SerDes)
- Custom Digital
- Analog/RF
Totem: Core Technologies

Extraction
- On-chip PG RLC + Substrate RC extraction
- EM aware extraction

Analysis
- Support for complex analog and mixed signal designs
- Transient analysis with ps resolution
- EM/ESD analysis for advanced technology nodes

Modeling
- Transistor-level macro models
- Multi-cycle Multi-mode models
- Model roll up to SoC

Extraction:
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Modeling:
- Transistor-level macro models
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Totem Analysis Flow

1. **GDSII**
   - Vector Simulation
   - Signal Only Net-list

2. **Design Modeling**
   - PG grid view
   - Current/Capacitance model

3. **PG Extraction + Simulation**
   - Totem Internal Model

4. **GUI Based Debug**
   - Layout Annotated Results
Grid Weakness Check
Resistance Bottleneck

- Grid weakness map is the normalized resistance of all transistor pins in the design
- Highlight weakly connected transistors
Case Study: Analog IP

Layout View

Analog Supply IR Map

Gross Connectivity Issue

Metal3 strap not extended

Early layout analysis helps catch gross grid violations
Dynamic Voltage Drop

- Worst IR drop of transistor pins shown
- Cross probe a list of transistor pins with the layout
- Plot the currents/voltage of all transistors based on list
Substrate Noise Coupling

Device Level
Threshold voltage modulation

Circuit Level
Functionality / performance issues in Analog & RF circuits

System Level
Preventing integration of sensitive circuits

Check/Sign-off Full-chip Noise

Plan/Analyze Isolation Structures

Check Noise Impact on Delay

Digital Core
PLL
Memories

Threshold voltage modulation
Functionality / performance issues in Analog & RF circuits
Preventing integration of sensitive circuits

Check Noise Impact on Delay
Chip Image Sensors: Key Challenges
Chip Image Sensors: Key Challenges

Noise Coupling
- Digital Switching Noise
- PG Grid Coupling
- Substrate Noise Coupling
Chip Image Sensors: Key Challenges

Noise Coupling
- Digital Switching Noise
- PG Grid Coupling
- Substrate Noise Coupling

Power Noise Analysis
- Digital Logic (Vectored/Vectorless)
- Analog (Vectored)
- Substrate Noise (Digital + Analog)
RF/Analog Design

Support for Complex Structures:
- BJT
- Diodes
- Poly R/TiN
- Metal R
- Mim/Mom Caps

BJT Device: Entire PNP Structure:
- Emitter
- Base
- Collector
- Pdiff
- Ndiff
- BJT marker Layer
Case Study: RF Analog Power EM

Schematic of RF/Analog Part of Chip

M3/M2/M1 Layout View

M3/M2/M1 EM Map

Narrow M2 straps carrying significant current causing EM violation
Memory and Custom Digital Designs
Complete Sign-off Flow

Coverage/Weakness Detection

Power Analysis
- Static DC

Signal EM Analysis
- VectorLess Transient

Sign-off
- Vectored Multi Cycle Multi State
- Vectored Multi Cycle Multi State
Large Design Handling

- Full-chip capacity
- Large DRAM memories
- Large FLASH memories
- Embedded Big Analog, Small Digital blocks

<table>
<thead>
<tr>
<th></th>
<th>Small Design</th>
<th>Large Design</th>
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<tbody>
<tr>
<td>Node Count</td>
<td>14M</td>
<td>321M</td>
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<tr>
<td>Transistor Count</td>
<td>7M</td>
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<td>Run Time</td>
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<td>20h22m</td>
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IP Modeling and Sign-off for SoC

IP/Block Design Sign-off

Model Creation

IP Enabled Full Chip Sign-off

Totem

IP/Block IR, DvD, EM, ESD Sign-off

Physical + Electrical

Embedded Constraints

IP Protection

IP Boundary condition Sign-off

Full-chip DvD/EM/ESD Sign-off

RedHawk
Case Study: IP Modeling

- Xtor Level Voltage Drop of Mem1 (WRITE)
  - Worst xtor drop ~ 210mV

- Xtor Level Voltage Drop of Mem2 (READ)
  - Worst xtor drop ~ 130mV

Two instantiations of same memory macro

SoC instantiating the hierarchical models generated using Totem
Totem: Power-Noise-Reliability
Custom, Analog & RF Designs

Coverage
Mem/SRAM
DDR/Serdes
TCAM/DRAM
Analog/RF

Noise
IR Drop
DvD
Substrate Noise

Reliability
Power EM
Signal EM
ESD

Usability
Versatile GUI
Layout Based
Full-Chip Capacity