Thermal Reliability for FinFET and 3D-IC Designs

Design Automation Conference 2014
Technology Trends and Thermal Challenges

Higher Integration on 3D-IC
- Thermal Interaction on Chips

Increasing Gate Density
- Elevated Thermal Impact

Higher Drive Strength Devices
- Higher EM(T) Impact

Shift from Planar to FinFET

65nm → 40nm → 28nm → 20nm → 16nm
Thermal Reliability

- EM (Electromigration) is the gradual displacement of metal atoms due to high current density
  - Causing open/short circuits

- High temperature (T) accelerates EM, a thermal reliability issue
  - Limiting allowable current density

- On-chip Tmax control and thermal run-away avoidance
Impact of Self-heating on FinFET

- Higher temperature on FinFET expected
  - For smaller Lg or higher Fin height, Max. Temp increased
  - 3D narrower fin structure and lower thermal conductivity in substrate causing heat trap
- 25°C increase on FinFET degrades expected lifetime by 3x to 5x on device and metal layers
- How to estimate temperature rises?
  - FEOL (devices), BEOL (wires), and their thermal couplings

Fig. 8. Impact of scaling gate length and fin height on the self-heating behavior. The figure shows the following: 1) ETSOI device has a smaller temperature rise as compared to FinFET device, and 2) fin height scaling in FinFET device (similar to active area scaling of ETSOI) and gate length scaling can counterbalance the self-heating effect.

SHRIVASTAVA et al.: INSIGHT TOWARD HEAT TRANSPORT AND MODELING FRAMEWORK, IEEE TRANSACTIONS ON ELECTRON DEVICES, 2012
Thermal Coupling Due to Self-Heating

\[ Wire \Delta T_i = \sum \Delta T_{ij} \] from both FEOL and BEOL self-heating

FinFET devices with self-heating
Function of Rth, finger number, fin number, Power

FinFET heating
Silicon Substrate

BEOL wire self-heating couplings
Function of Width, Irms, Layer
Thermal Coupling Effects in BEOL

Thermal coupling between wires

Distance from heat source

T-Decay Rate

ΔT

6/23/2014
Self-heat Flow in RedHawk/Totem

Tech file / LIB / Dev Models

DSPF w/ Signal RC

LEF/DEF/GDS

Foundry SH Input

RedHawk

Totem

Power EM Run → CTM
P/G wire lavg info

Signal EM Run → Signal wire Irms info

Self-heat calculation including thermal coupling

Inst Self-heat Report

Wire Self-heat Report

Thermal Profile / Back-annotation
Example Metal Layer Temperature and EM Maps

Temperature

Heat Flux

17: TOP_LAYER
16: metal7
15: via6
14: metal6
13: via5
12: metal5
11: via4
10: metal4
9: via3
8: metal3
7: via2
6: metal2
5: via1
4: metal1
3: device_2
2: device_1
1: Substrate

M2 Temp Map

Signal EM (M2) Map
Chip Thermal Interaction on 3D-IC

- Thermal sensor in DRAM cannot monitor the Hot-spot accurately.
  - Thermal gradient may cause refresh error.

Refresh Control Issue

- SoC hot spot affects the DRAM by the thermal coupling

**Top View**

- Cross section
  - DRAM
  - SoC

- DRAM layers
- SoC layers

- Refresh Error

- ΔT = 22.4°C
- High refresh rate is required

FEM analysis results (Temperature contours)

- Image Sensor thermal analysis Lid, die, wires, metals, solders modeled in Sentinel-TI

Courtesy of Renesas in 3D-ASIP, 2013
Chip-Package-System Thermal Solution

IC Simulation for Thermal-aware EM
(RedHawk/Totem)

CTM

Temperature Maps

3D-IC Chip/Pkg Simulation
(Sentinel-TI)

Power Maps

Thermal BC

System Simulation
(Icepak)

Chip-aware System Thermal Analysis

System-aware Chip Thermal EM Analysis

Chip Thermal Models
On-chip Thermal-Aware EM Flow

Black’s equation for mean-time-to-failure (MTTF):

\[ MTTF = A J^{-n} e^{\frac{E_a}{kT}} \]

Temp increase causes EM limit decrease.
Transient Thermal Responses
*Due to High/Low Power Mode Switching*

Power Mode Sequence in Time

\[ T(x, y, z, t) = \int_{0}^{t} T_s(x, y, z, t - \tau) \frac{\partial P(\tau)}{\partial \tau} d\tau \]

\[ \Delta T_{JA}(t) = \]

\( T \): Temperature results

\( T_s \): Temperature response for power on, a step change

\( P \): Power (map) on chips

- Optimize thermal sensor placement
- Accurate Tmax determination
Thermal Integrity Coverage

On-chip FinFET Delta-T
- Measurement-based FEOL/BEOL Delta-T formula for device/wire self-heat
- Simulation-based thermal coupling between wires

SoC / 3D-IC Tmax
- CTM-based thermal analysis on chip-package-system
- Good silicon correlation

On-chip thermal-aware EM
- Thermal-aware EM flow needed for tight EM margin on advanced technologies
- Thermal related reliability check is a must
Summary

- FinFET thermal reliability analysis requires accurate and fast thermal simulations
- FinFETs require BEOL and FEOL thermal coupling modeling for accuracy
- Chip-aware thermal analysis required for accurate package/system analysis
- System-aware thermal analysis required for accurate on-die temperatures
- Thermal-aware EM is mandatory for FinFET class designs