Designing Robust Electronics Systems

Parametric simulation and high-performance computing ensure that engineers develop reliable electronic serial interconnects.

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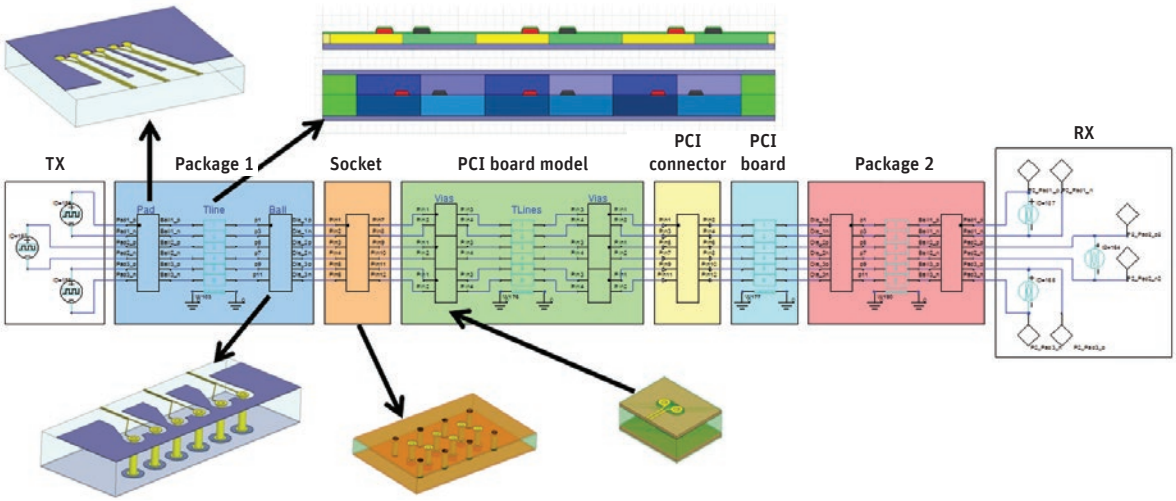
In the electronics industry, R&D teams often use extensive numerical simulation to explore device performance. Simulation provides an understanding of components and systems that laboratory tests are unable to deliver — in some cases, physical testing is not even considered as an investigative tool. It is possible to simulate an entire system early in the design cycle and to explore issues and parameter values to identify likely sources of system failure, long before they are locked into the design. Modern simulation methods take advantage of advanced computing hardware and novel numerical methods.

Engineers who design computer servers, storage devices, multimedia PCs, entertainment systems and telecom systems are driving the industry trend to replace legacy shared parallel buses with high-speed, point-to-point electrical interconnects. Standard interfaces, such as XAUI, XFI, Serial ATA, PCI Express®, HDMI® and FB-DIMM, have emerged to provide greater throughput using serial signaling rates of 2.5 Gb/s to 10 Gb/s. While this trend has greatly reduced the number of traces and connections within the system, it has created new challenges for electronic system designers who must consider implementation with multiple connectors, transmission lines, vias, IC packaging and transceiver circuits. Very high speeds require the use of advanced, full-wave electromagnetics simulation techniques to capture the interconnect's behavior.

SIMULATING THE PCI EXPRESS CHANNEL

PCI Express (peripheral component interconnect express) is a high-speed serial bus standard used in virtually all PCs to connect the motherboard to expansion cards and add-in boards. This high-speed interface sends digital signals across a collection of individual components. Signals travel from the transmitter (TX) to the receiver (RX) by traversing the IC package, IC socket, PC board, PCI connector and board, and second IC package. Each component can disrupt the signal as it propagates from transmitter to



▲ PCI Express channel containing transmitter, BGA IC package, socket, printed circuit board, PCI connector and board, another IC package, and receiver

receiver. Engineers design components to minimize signal reflections and losses to achieve reliable communication. To do this, the engineer must understand how all of the components interact with one another within the full system.

Each component has its own set of tunable parameters. A transmission line on the motherboard, for example, has several parameters including trace width, thickness and spacing between traces; dielectric constant for the substrate; substrate thickness; and trace manufacturing defects, such as over- and under-etching. Another common component is a printed circuit board (PCB) via structure that allows circuit traces to traverse from one layer to another. Such a via structure with associated electric and magnetic fields can be simulated using ANSYS HFSS. The geometry has numerous parameters, including substrate thickness, dielectric constant, routing configuration (input layer, output layer), via barrel thickness, pad diameter, anti-pad diameter and via stub length. Considering all of the components in the interconnect (as shown in the illustration), there could be 30 or more parameters that affect performance if all the possible variations are included. The engineer varies these parameters over a prescribed range to optimize the design for performance. Of course, each of these parameters has specific manufacturing tolerances, which is especially important considering that numerous vendors may be selected to supply materials and components. The challenge to the engineer, therefore, is to find a suitable design within the design space that is simultaneously robust to design variations and manufacturing tolerances.

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It is easy to illustrate the vast solution space that can develop when each of the parameters have several values. For example, if each of 30 parameters has three values over some prescribed range, then the total number of possible combinations is 3^{30}, which is more than 200 trillion! It isn't possible to measure all of the combinations. Even powerful simulation capabilities cannot provide complete coverage of such a vast solution space. To address this issue, a popular technique is to apply design of experiments (DOE) and response surface modeling. Response surface modeling enables the designer to model and consider all aspects of a high-speed channel design by fitting a statistical model to outputs of the simulation as a function of changes in input variables. A DOE table is used to select design points to solve to build the statistical model. Optimized conditions and worst-case scenarios are obtainable within the set of all possible design combinations.

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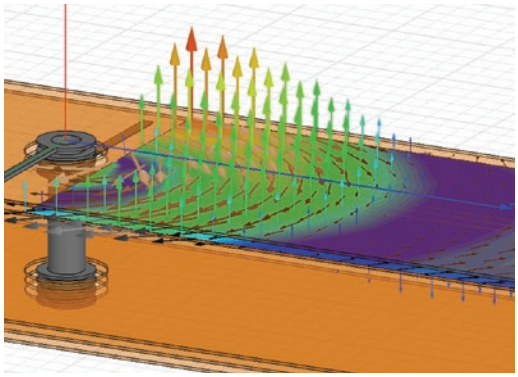


▲ Electric and magnetic fields surrounding PCB via structure as simulated by ANSYS HFSS

Advanced numerical simulation coupled with high-performance computing allows engineers to simulate complete products and to fully explore the design space.

SIMULATION PROCEDURE FOR DOE

To apply the DOE method to this high-speed interconnect example:

Step 1: Assemble the PCI Express channel using a systems-level simulation tool (ANSYS DesignerSI). Link this channel to electromagnetics models for all components (BGA package, connectors, printed circuit boards, etc.).

Step 2: Select variables for the DOE study and associated output observables. In this case, the outputs are selected to be eye-diagram height and width.

Step 3: Launch ANSYS DesignXplorer and set the variable range.

Step 4: Create a DOE table in DesignXplorer. The table is then passed to DesignerSI, and the full parametric simulation is performed. The distributed solve option (DSO) license accelerates simulations by running multiple parameters simultaneously on a compute cluster.

Step 5: Circuit simulation results from DesignerSI are passed back to DesignXplorer. DesignXplorer produces a statistical response surface model. Plots of sensitivities and six sigma behavior can be analyzed.

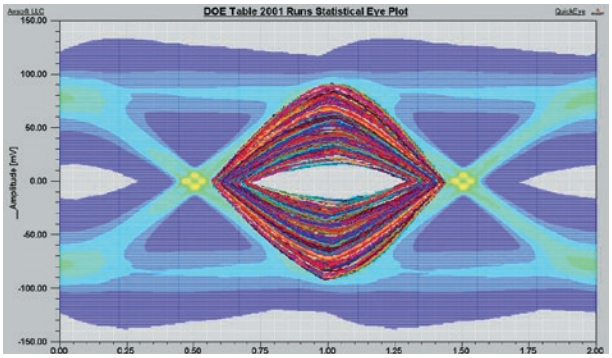
For this example, engineers used DesignXplorer to set up a DOE table requesting 2,001 independent simulations to be run in DesignerSI for the PCI Express channel. For each of these 2,001 simulations, parameter values were selected across a range as specified by the user, but the unique combinations of those parameters were set up automatically by DesignXplorer to obtain statistically independent results. To solve the scenarios required quickly, DSO with ANSYS Designer was employed. Eight parallel solves were performed at a time, taking advantage of all eight cores on a desktop server.

One useful graphical technique is to employ DesignerSI to produce an eye diagram of the signal as observed at the receiver. A broad sequence of digital signals is sent by the transmitter with switching events occurring to represent a digital one or zero, representing either a high- or low-voltage signal. Combining these simulated switching events one on top of another results in an eye diagram. An open eye with large eye height and width is an indication that a received signal can be detected reliably. A closed eye means that the signal swing and speed are insufficient for reliable detection.

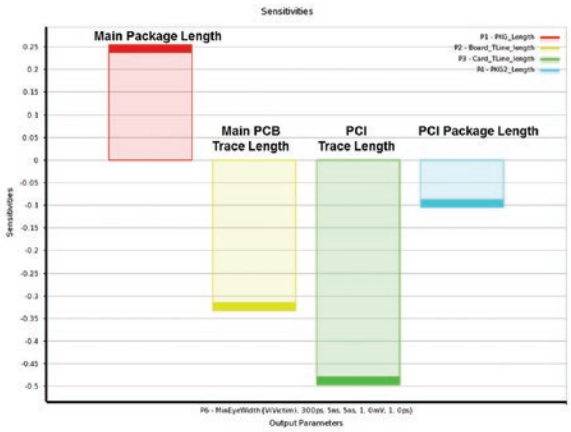
The eye diagram represents the behavior of the PCI Express channel when a large number of bit sequences have been sent through the channel. It also shows the result of varying a subset of the 30 parameters over a collection of 2,001 trials, as set up in the DOE table. Some combinations of parameters result in a substantially closed eye, indicating a poor design point. A complete response surface for eye height and width can be generated,

Component	Associated Parameters (Numbered)
Package	Thickness, pad breakout, trace length, solder ball pitch, dielectric material (5)
Socket	Thickness, material properties, signal-to-ground ratio (3)
Board	Microstrip and stripline trace and spacing, etch factors, Cu roughness, dielectric material, via configuration (8)
Connector	Various vendor models, often only one or two options (1)
Second Board	Microstrip, stripline, etch factors, Cu roughness, dielectric material, via configurations (8)
Second Package	Thickness, pad breakout, trace length, solder ball pitch, dielectric material (5)

▲ Components in a typical PCI Express interconnect may have 30 parameters or more.



▲ Eye diagram resulting from large parametric sweep of example PCI Express channel. An eye diagram is used by engineers to determine if a digital signal can be received accurately. An open eye indicates that the interconnect has good performance.



▲ DOE results for several significant parameters in PCI Express interconnect simulations. The PCI trace length on the peripheral card had the greatest negative impact on the eye opening, followed by the main PCB trace length.

providing the engineer with information about which parameters have the greatest positive or negative effect on interconnect performance. The engineer can obtain DOE results for several significant parameters in PCI Express interconnect simulations. The PCI trace length on the peripheral card had the greatest negative impact on the eye opening, followed by the main PCB trace length. Engineers can use this analysis to detect the most significant parameters on system performance. In this case, a more careful selection of the PCI peripheral card design and/or materials to reduce losses would improve this design.

LEVERAGING SIMULATION-DRIVEN DESIGN

Advanced numerical simulation coupled with high-performance computing allows engineers to simulate complete products and to fully explore the design space, such as with high-speed serial interconnects. Simulation makes it possible to create a virtual prototype of the system so that design analysis, parametric variations and optimization are performed before costly and time-consuming prototyping, lab tests and production. In the past, simulations could support only a single physics, a single user, a single component, and just a few design points. With today's modern high-performance computing hardware and software, it is possible to leverage a Simulation-Driven Product Development approach to include multiple physics, circuit and system simulations, and multi-user, multiscale simulations with parametric optimization and design exploration.

Reliable HPC Solutions for Electromagnetics Simulation

To enable robust design, HPC methods allow large electromagnetics studies to be distributed across a network of computers (cluster) to solve large 3-D volumetric problems, to perform material and geometry parametric sweeps, and to solve across frequency.

DOMAIN DECOMPOSITION

The domain decomposition method (DDM) distributes a simulation across multiple, potentially networked cores to solve large, complex problems. DDM generates a continuous finite element mesh over the entire structure, then subdivides that mesh and uses a distributed-memory parallel technique to distribute the solution for each mesh subdomain to a network of processors. This substantially increases simulation capacity. Domain decomposition is highly scalable to large numbers of processors and takes advantage of multithreading within the mesh subdomains to reduce solution times for individual subdomains.

SPECTRAL DOMAIN DECOMPOSITION

The spectral decomposition method (SDM) distributes the multiple frequency solution over networked compute cores to accelerate frequency sweeps. You can use this method in tandem with multithreading, as multithreading speeds up extraction of each individual frequency point, while spectral decomposition performs many frequency points in parallel. The spectral decomposition method is scalable to large numbers of cores, offering significant computational speed. SDM technology is available with ANSYS HFSS, HFSS-IE and Apache's Sentinel PSI.

DISTRIBUTED SOLVE

The HFSS distributed solve option (DSO) accelerates sweeps of design variations by distributing design iterations across a network of processors. It works synergistically with multithreading to increase the execution speed of each design iteration. HFSS DSO offers a near-linear speedup over conventional design sweeps and is scalable to large numbers of cores.