

Thermal Coupling of On-chip Hot Interconnect for Thermal-aware EM Evaluation

Driven by mobile computing and communications, the SoC have been growing very rapidly in silicon integration technology scaling, advanced low power techniques while meeting higher performance requirements using a variety of packaging technologies. The internet of things (IoT) is opening up new applications with connected devices and systems, where low power, high performance and reliability are paramount. Since the impact of temperature on power, performance and reliability is huge, accurate thermal analysis is a requirement for the design flow.

In advanced process technologies such as FinFET or FDSOI, the wire width and spacing are reduced and the current density is increased, leading to increase in wire temperature (ΔT) on wires. Typically, this is due to self-heating and thermal coupling among wires, and can impact the chip's reliability and performance. Power due to self-heat is defined as I^2R , where I (current) can be I_{AVG} on power/ground wire or I_{RMS} on signal wire. A traditional methodology uses uniform worst-case temperatures across the chip for electromigration (EM) sign-off. This method is not only pessimistic, but also fails to take thermal hotspot into account. Therefore estimating the realistic temperature of wires is necessary for ensuring reliability while optimizing the wire design. Due to the large number of wires in a modern chip, applying direct thermal field solution such as Finite Element Method (FEM) across all wires is not feasible. This paper describes an innovative method for efficiently and accurately calculating the impact of self-heat related temperature increase on millions of wires. Also outlined is the thermal-aware EM methodology that considers both self-heat and the chip-package-system (CPS) thermal environment.

Wire temperatures of a chip are critical data that are used to determine the allowable currents on wires that meet the expected Mean-Time-To-Failure (MTTF) as described in Black's equation (Figure 1). This is used to predict EM reliability failure of a metal wire, which over time result in undesired open or short circuits. Wire/device temperature impacts power (particularly leakage power, which is an exponential function of temperature), resistance, EM limit, and consequently EM, IR/dynamic voltage drop, signal integrity, ESD, and timing.

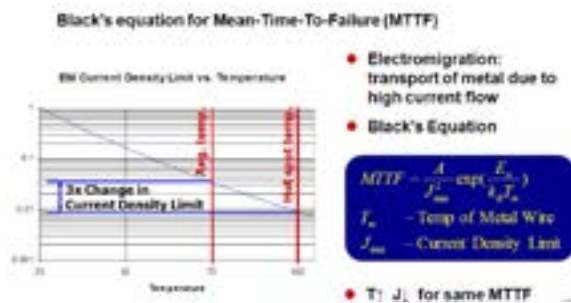


Figure 1. Thermal impact on electromigration

Accurate estimation of the steady-state temperature of a wire over thousands of clock cycles requires the following inputs:

1. Power of CMOS devices when they are in actual operating state (i.e. switching or idle mode)
2. Thermal environment of a chip in a package such as thermal conductivity distribution, including multi-die heating for 3D-IC design, and variations of the CPS configurations
3. Self-heat component of a wire, which is typically caused by thermal coupling between wires and power dissipation from the average or root-mean-square (RMS) current that flows through the wire.

Typically, the device heating is the dominant part of a chip's total power consumption. Chip-level power analysis tools such as ANSYS RedHawk or Totem generates Chip Thermal Model (CTM) which represents impact of device heating in terms of fine grid power maps. ANSYS Sentinel-TI is a FEM tool that models and solves thermal profiles of a chip(s) in IC package such as 3D-IC. The model uses CTM power as well as system thermal boundary conditions from a board-level CPS analysis or a system-level thermal analysis using ANSYS Icepak, a system-level thermal solutions using Computational Fluid Dynamics (CFD) simulation. CTM contains total power of a chip. This includes temperature-dependent leakage power on devices and metal distribution data of the interconnect layers.

Even though self-heating of wires in the chip's interconnect layers constitute a small portion of the total power, as the technology scales to 16/14 nm and below, both current density and electrical resistances on wires increase leading to significant rise in local self-heating and temperature. Since the number of wire segments on a chip is usually in the multiple millions, it is difficult to solve self-heating using a field solver such as FEM or CFD. RedHawk and Totem uses a novel and efficient approach to calculate the wire's temperature rises as well as the thermal coupling effects. For accurate EM analysis the base temperature from CTM flow is used together with the temperature rise on wires, which are calculated using the novel approach that includes wire self-heating and thermal coupling.

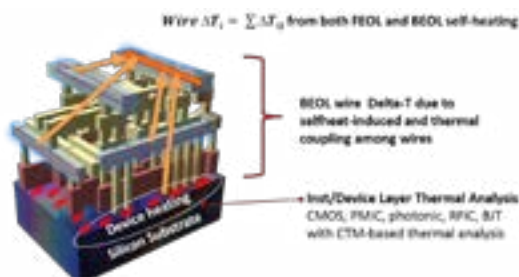


Figure 2. Thermal coupling due to self-heating on devices and wires.

Thermal coupling due to self-heat on devices and wires is illustrated in Figure 2. The increase in self-heat (ΔT) of each Back End of Line (BEOL) wire buried in a dielectric media is pre-characterized using ANSYS Mechanical, a general purpose FEM tool. The pre-characterization process takes geometry and physical factors into consideration. These factors include current, electrical resistance and geometry of the wires, thickness of the dielectric layer, positioning and thermal conductivity of the dielectric, and content of the neighboring metal. Temperature decay behavior in the dielectric is a key component in the calculation of thermal coupling among wires. With ΔT and temperature decay characteristics, the thermal coupling among wires is readily and efficiently calculated using linear superposition method.

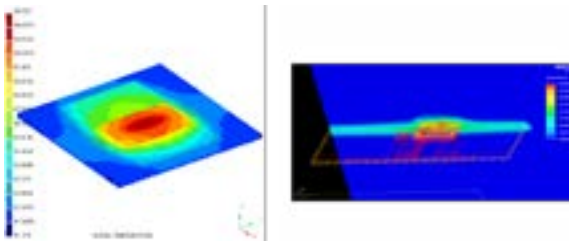


Figure 3. 3D-IC package (right) in CPS environment with thermal boundary condition from CFD (left)

CPS thermal simulation results of a 3D-IC using Icepak generated boundary conditions is illustrated in Figure 3. An FEM and/or CFD field solvers are used for thermal convection and radiation outside the conductive solid boundaries of CPS. The final thermal-aware EM analysis is performed using fine wire resolution (Figure 4) and temperature levels compatible to a realistic CPS environment. This method allows designers to easily identify and fix wires with high EM limit violations during the chip design sign-off flow.

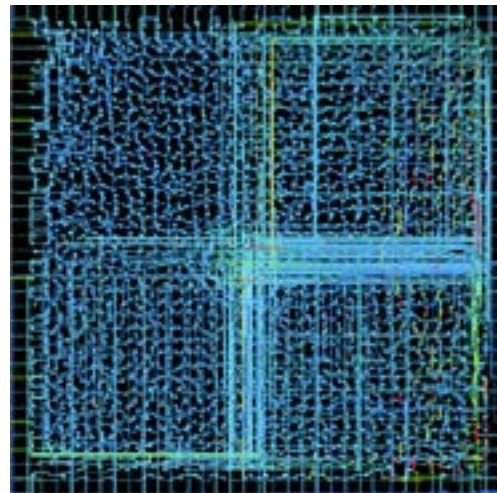


Figure 4. EM limit percentage on signal wires with CPS thermal environment and wire self-heating considerations

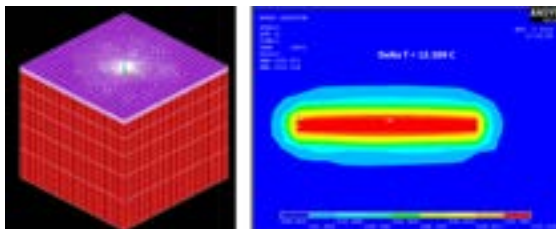


Figure 5. 3D finite element model for characterizing temperature rise of a wire in dielectric layers

In the self-heat pre-characterization process, FEM is used to create detailed 3D modeling of a wire in dielectric layer on silicon substrate. An example of the analysis model and the typical temperature profile of a wire, including the decay profile into the dielectric media are illustrated in Figure 5. This type of simulation serves as the base for efficiently predicting the temperature rise on each wire with a given wire geometry and environment configuration. The temperature decay behaviors for the above simulation are characterized using models similar to those in Figure 6. Thermal coupling among the wires is obtained by using wire arrays with the parameters for wire sizes, pitches, elevations/locations of the heating wire, and decay directions. The thermal coupling results show the temperature rises due to the self-heating in wires. Reliability of wires is a function of the final temperature of a chip, which is a function of the thermal influence across chip-package-system using temperature-dependent CTM power maps. After iterations in the CPS environment, the temperature and power converge, showing consistent temperature profile and power map (Figure 7). For multi-chip and 3D-IC designs, CTM and CPS approach provides convergence of on-chip temperature profiles simultaneously. The converged thermal profile combined with wire thermal coupling deliver a complete solution for thermal-aware EM analysis.

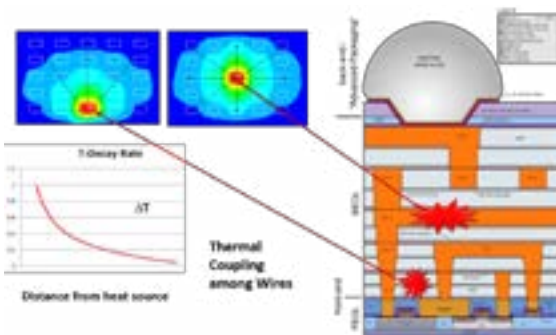


Figure 6. Temperature decay from wire with self-heating embedded in dielectric layers

The base temperatures on layers and wires due to device or Front End of Line (FEOL) heating (Figures 2 and 7) are calculated using CTM based thermal analysis (Figure 3).

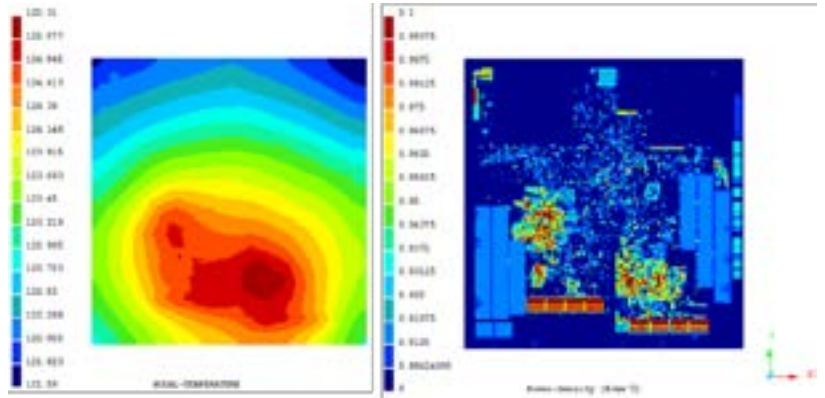


Figure 7. FEOL device power from CTM (right) and thermal profile on chip layers as base temperature for wires

In summary, with advanced process technologies including FinFETs, as the density of SoCs increase, so does the thermal-induced electromigration within the chip, which is a major reliability issue. Instead of applying the traditional uniform worst-case temperature based methodology, ANSYS has developed an innovative technique that uses the self-heat-induced ΔT and Thermal coupling of wires for accurately and efficiently calculating the wire temperature of the hundreds of millions of nanometer wires in a SoC today. ANSYS offers a thermal-aware EM methodology that uses both self-heat and chip-package-system thermal environment enabling designers to create the most reliable ICs for markets such as mobile, communication and automotive.

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