Chip–Package–System (CPS) Co-design and Thermal Management of Electronics

Dimensions of Electronic Design Seminar
Agenda

• Trends Driving Chip-Package-System Co-design
• ANSYS/Apache Synergy for Chip-Package-System Enablement
• Co-Design Case Studies
  – PI: Power delivery analysis & optimization
  – EMI: Near field and far field radiation analysis with design feedback
  – Thermal: thermal reliability and stress analysis of 3D-IC
  – SI: SSN analysis & optimization
Power Efficiency for Complex Electronics

Mobile / Consumer
- Performance
- Power Efficiency

Automotive / Medical
- Reliability
- Interference

Computing / Communications

Aerospace / Defense
System-Level Analysis Coverage

- Power Integrity
- Signal Integrity
- Thermal Reliability
- Electromagnetic Interference
Components in Electronics Systems

- **Chip**
  - On-chip decoupling
  - Die parasitics
  - Current/Power signature
  - Bump map

- **Package**
  - Plane shapes
  - Discrete decoupling
  - I/O routing
  - Ball map

- **PCB**
  - Channel/SSO Analysis
  - Multi-domain
  - EMI Due to Current Signature

Printed circuit board (PCB) with multiple package chips
Chip inside package
Trends Impacting CPS Power Integrity

**Die-level Challenges**
- Ultra-low power, 100+ Domains
- Reduced noise margin
- Multi-GHz performance
- Multi-Core
- 3DIC integration

**Package/PCB Challenges**
- Cost down: fewer layers, caps
- Reduced target impedance
- Thermal reliability/stress
- System resonance
Requirements for Electronic Systems: High Performance

Challenges
- SoC designed for 2GHz

However:
- System only reached 1.2GHz due to package/chip resonance

Simulation Requirements
- Model full chip/package/board supply system
- Model excitation from chip through package and PCB

“... optimizing chips to work at near threshold voltage levels and 3D-IC packaging will be needed to lower memory power ...”

Intel, EETimes, 2/20/2012


Chip Pad Supply Voltage W/ and W/O Resonance Conditions
Requirements for Electronic Systems: **Power/Thermal Management**

### Thermal Challenges
- Close proximity of electronics creates cooling challenge
- Heat transfer from adjacent chips
- Materials with high thermal conductivity may be used (and need to be modeled in analysis)

### Simulation Requirements
- Chip Thermal Model
- Thermal Boundary Conditions
- Package/PCB Thermal Modeling

we’ll be asking industry to focus ...on how do we make these things faster, how do we hook them up end-to-end and ensure that we remove heat efficiently, that we handle a lot of power. When you’re generating a powerful jammer ...it’s all the more important that you be able to handle large amounts of power and heat.”

Capt. John Green, NAVAIR PMA-234 commander

Source: Avionics Magazine, Sept. 2010
Average semiconductor content of automobile increases 15% per year
  • EMI is a key safety concern
  • Traditional EMI modeling neglects core noise

Simulation Requirements
  • Chip emission modeling (core, I/O)
  • Package/PCB/cable radiation analysis

Increasing need to predict the true post-silicon EMC behavior vs. *increasingly aggressive EMC targets* dictated by marketing, customers, and international standards

Dr. Davide Pandini, ST Microelectronics, Agrate, Italy

ST Microelectronics, Doriol et al., DAC 2009
Enabling Electronic Systems through Chip-Package-System (CPS)

Unified ‘model-based’ design simulation environment
- Chip aware package-PCB-system simulation
- System-Package-PCB aware chip simulation
ANSYS-Apache: CPS Solutions

End-to-End Chip-Package-System
Power, Thermal, EMI, Timing Platform

CHIP
RedHawk, Totem, PowerArtist, PathFinder

PACKAGE
HFSS, SIwave, Q3D, TPA, Sentinel – NPE, PSI, TI
Icepak, Mechanical

BOARD
SIwave, HFSS Q3D, DesignerSI, Icepak

CONNECTOR
HFSS, Q3D
System-aware IC Power Integrity

Q3D
Sentinel-NPE
RedHawk Package Compiler
RedHawk Totem

Dynamic Voltage Drop  In-Rush Current  Electromigration  ESD  3D-IC
Case Study : System-Aware IC Analysis

Full CPS Analysis

32nm CMOS Design

Transient Analysis

Without Package

With Package

AC Analysis

Chip, Pkg, PCB Impedance

Power integrity analysis results (time and frequency domain) vary greatly when the complete system is considered.

Source: Ciena, DAC 2012
Apache Chip Power Model (CPM)

- Spice-format model of the on-chip power distribution system (PDN)
- Captures PDN impedance and switching current profile

Group definition

[Diagram showing block definitions and waveforms]
CPM Overview

Analysis Mode
- Static ($I_{avg}$, $R$)
- Frequency Domain (RLC)
- Time Domain ($I(t)$, RLC)

Model reduction
Early CPM Generation: RTL2GATE

Why RTL2Gate Power?
- Consistency
- Coverage
- Flexibility

RTL Analysis
~ Million Cycles

Physical Design
~ 20 cycles

System Design

RPM

CPM

PowerArtist

RedHawk

Sentinel

SIwave

CPM(Layout)+Pkg
CPM(RPM)+Pkg
Pkg only
Chip Aware System Power Integrity

RedHawk Totem

CPM (Chip Power Model)

Slwave

Sentinel-PSI

Chip Power & Emission Model

DC IR-Drop

AC Analysis

Dynamic Voltage Drop Analysis

EMI/EMC
PDN Analysis in Whole System

System AC Simulation

Capacitor placement

Time domain system analysis

PDN Analysis in Whole System

Capacitor in package

Capacitor in board

CPM

BGA Package

Bulk capacitor

VRM

Power Line

GND Line

Red: Original (no pkg decaps)
Yellow: 4 pkg decaps, each 220nF, 300pH ESL
Green: 4 pkg decaps, each 47nF, 105pH ESL

Idle transition

Active

w/o pkg decap (192mv)
w/ 1/2x pkg decap (68mv)
w/ original pkg decap (68mv)
Chip-Package-System Co-simulation

- Chip-Pkg-System Co-Simulation
  - The real operated noise source of IC is applied

The waveform of supplied power and ground.

Transient analysis

Package & Board Analysis Models

PCB+Pkg

SIwave

ANYS DesignerSI™ with Nexxim®

Apache CPM
3D-IC: CPM-based Versus Concurrent Analysis Two Die TSV Test Case

Concurrent Approach

CPM Based Approach

Schematic of Simulation Setup

Voltage map for top die
ANSYS-Apache CPS EMI Flow

CPM

→

HFSS/Siwave/Sentinel-PSI

→

Near/Far Field Radiation
CPS EMI Simulation

Chip-aware System EMI Analysis

CPM from RedHawk

Sentinel-PSI Package EMI Map

Smartphone EMI Simulation in HFSS

IC-level EMI Hotspot Analysis

2nd harmonic

5th harmonic

RedHawk: EMI Source Maps

Noise Spectrum
Factors Impacting CPS EMI Analysis

- Higher electronic content
- Increased regulations
- High speed devices

Chips are the EMI Source
Pkg/PCB form the Antenna

EMC envelope
Failure!
Case Study: EMI Over Range of Frequencies

Displays EMI movie for the range of specified frequencies, for power nets.

Highlights the HOT Emission Regions at Various Frequencies.
Chip and System-level Thermal Co-analysis

**Chip Thermal Model (CTM)**

- **Accurate chip power distribution for system level thermal analysis**
  - Chip Thermal Model (CTM) generated from **RedHawk** full-chip power analysis
  - CTM-converged power/thermal map generated by **Sentinel-TI**

- **System-level thermal Boundary Condition for Package thermal analysis**
  - Constant coefficients on package top/sides and board top/bottom generation in ANSYS Icepak
Die Layout-aware Power-Thermal Convergence in CTM-based Flow Considering Self-heating Power

CTM: Lookup power map from temperature map
ANSYS + Apache

IC-Aware System Thermal Analysis

RedHawk

CTM

Temperature Map

Sentinel – TI + Slwave

Conv. Power Map

Board current

Heat transfer coefficient

Icepak

Chip Aware Package and System Thermal Analysis

System Aware Package and Chip Thermal And Reliability Analysis
Factors Impacting CPS Signal Integrity

- **Drivers**
  - 1GHz+ (DDR3)
  - Supply voltage <1.0V

- **Simulation Considerations**
  - I/O ring noise
  - Package traces
  - PCB traces
  - Termination load
Chip Signal Model (CSM)
Signal Integrity Analysis & Optimization

Applications:
- I/O timing and noise targets
- Package/PCB design and optimization
- Chip Signal Model (CSM) creation for cross-domain analysis

Capabilities:
- Spice-based simulation with full IO bank (128+) capacity
- 3D full-wave package/PCB modeling
- P/G network inclusion

Models switching behavior & PG parasitics
Enables IP protection
Enabling ‘Converged’ Electronic Designs

Enable design prototyping
Identify errors early in the process
Reduce overall system cost
Overcome design boundaries

- Model Exchange
- Model Exchange
- Model Exchange
- Model Exchange

Architecture → IP → SoC → Package → PCB