SEMICONDUCTORS

Ansys Exalto

Electromagnetic Signoff Tool for High-speed RFICs and Digital SoCs

- **Enables accurate prediction of electromagnetic coupling effects during the signoff phase**
- **Identifies the root cause of unknown crosstalk, including electrical, magnetic, and substrate coupling**

Key Features

- Delivers unrivaled capacity and speed to solve even the most complex electromagnetic problems
- Analyzes circuits with thousands of ports
- Adds electromagnetic confidence to your signoff phase
- Reads encrypted foundry tech files
- Is optimized for silicon
- Supports many output formats for maximum efficiency in circuit simulation
- Is compatible with all IC design platforms, physical verification flows, and circuit simulators
- Is silicon-accurate

No Circuit Is Too Big to Analyze for Ansys Exalto

The unprecedented capacity of the electromagnetic modeling engine at the core of Ansys Exalto enables designers to analyze extremely complex layouts with ease. It helps predict electromagnetic coupling between sensitive RF circuitry and large digital buses or control signals in RFICs and digital SoCs built on the most advanced nanometer CMOS processes.

Exalto generates a fully coupled electromagnetic model for any combination of passive devices, arbitrary routing, layouts with planes (solid or perforated), MiM/MoM capacitors, and more. The model is then automatically back-annotated to the original schematic or extracted view of the design, thus accelerating post-layout circuit simulation. Extreme capacity and very fast modeling times with no compromise on accuracy, along with seamless integration in any physical verification flow, will shorten your signoff time and increase your confidence in the final product.

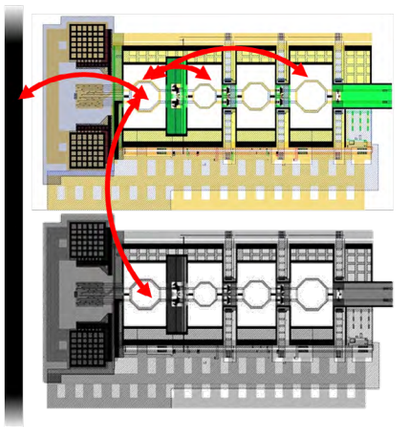

Figure 1. Various types of coupling that can be analyzed with Exalto, including stage-to-stage, block-to-seal ring, and block-to-block

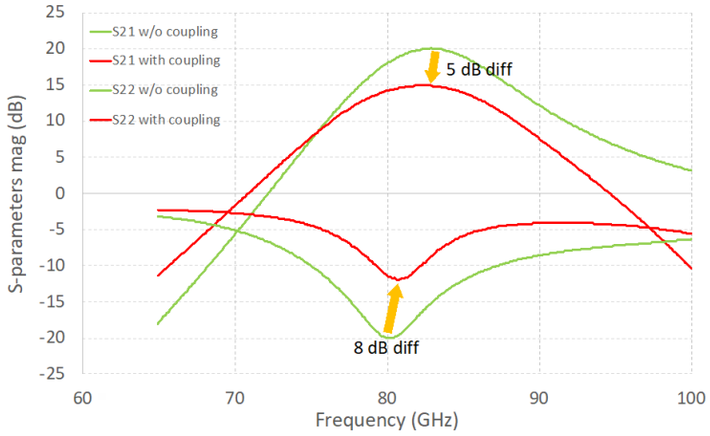

Figure 2. Significant deterioration of frequency response of 1 LNA block due to internal stage-to-stage electromagnetic coupling

/ Up to 300X Faster Signoff with the Electromagnetic Confidence of Exalto

The exploding costs of nanoscale silicon processes force design managers to come up with innovative design architectures, such as the placement of actives under or inside the white space of inductors. Risky design techniques that were considered “science fiction” a few years ago are now becoming the trend. To alleviate risk of failure and minimize costly re-spins, you need a very high-capacity and accurate electromagnetic modeling tool that can meet your toughest capacity demands under the tightest design schedules.

Combining the efficiency and unrivaled speed of Exalto with distributed execution shrinks the signoff phase from multiple days to a few hours. The new generation of Exalto delivers unprecedented levels of capacity, speed, usability, and the highest level of confidence in your simulations during signoff. This brings you many steps closer to first-pass silicon success.

/ Analyze Circuits with Thousands of Ports

Traditional electromagnetic solvers struggle as the number of ports that should be extracted increases. Exalto has solved electromagnetic problems with thousands of ports, proving that there is no limit to its capacity.

/ Silicon-proven Accuracy Down to the Most Advanced Process Nodes, With Coverage of All Layout-dependent Effects

Advanced process nodes introduce a multitude of challenges for electromagnetic solvers. Etching, multipatterning, conformal dielectrics, damage, and loading effects should be analytically calculated to produce an accurate electromagnetic model. Exalto is powered by the only electromagnetic solver that can guarantee the highest level of accuracy, as it fully models all layout-dependent effects in advanced CMOS process nodes.

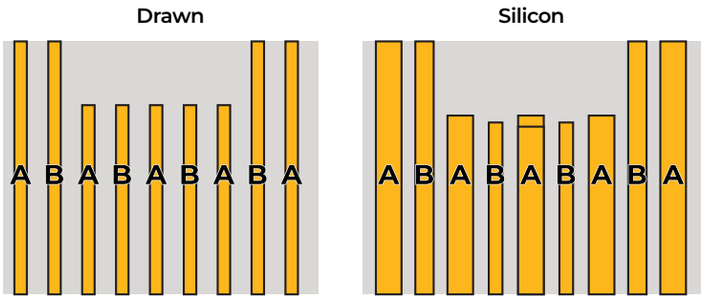

Figure 4. Multipatterning variation

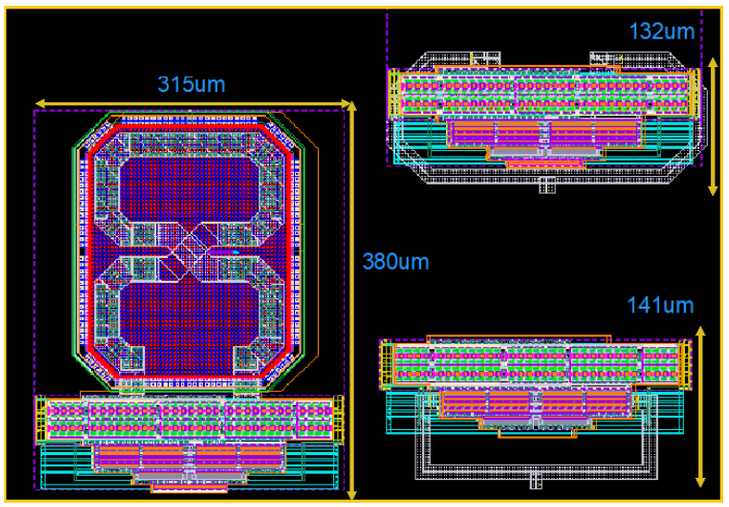

Figure 3. Traditional VCO architecture (left) and VCO architecture with inductor folded over capacitor bank (right)

Category	Description	Exalto
Conductor	Multi-patterning / Coloring	✓
Conductor	ETCHING (single or multiple tables)	✓
Conductor	Width dependent TC1/TC2	✓
Conductor	Metal thickness variation (Resistance)	✓
Conductor	Metal thickness and density bounds (Resistance)	✓
Conductor	Metal thickness variation (Capacitance)	✓
Conductor	Metal thickness and density bounds (Capacitance)	✓
Conductor	Sidewall damage thickness variation	✓
Dielectric	Constant damage thickness	✓
Dielectric	Bottom dielectric thickness variation	✓
Dielectric	Side dielectric thickness variation	✓
Via	RPV vs via area (Contact table)	✓
Via	RPV TC1/TC2 vs via area	✓

Table 1. Details of advanced layout-dependent effects modeled by Exalto

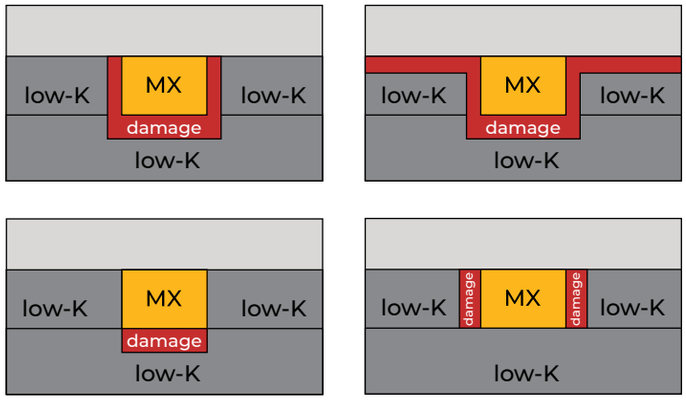

Figure 5. Types of dielectric damage

Multihost Electromagnetic Simulation

With its innovative distributed compute architecture, the is no capacity limitation for Exalto. Reduce the runtime, RAM footprint, and overall cost of your electromagnetic simulation by distributing your jobs on multiple small machines that are more readily available on your grid. Model huge areas of layouts many orders of magnitude faster than any other electromagnetic solver.

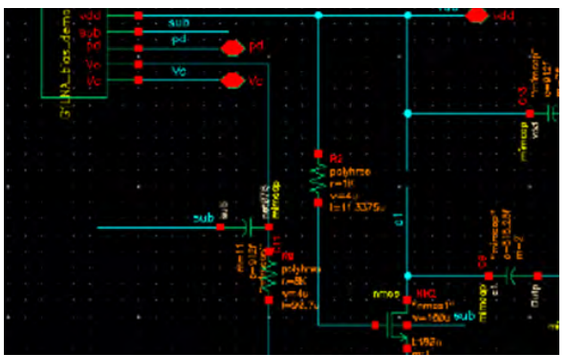

Figure 6. Simulation test bench

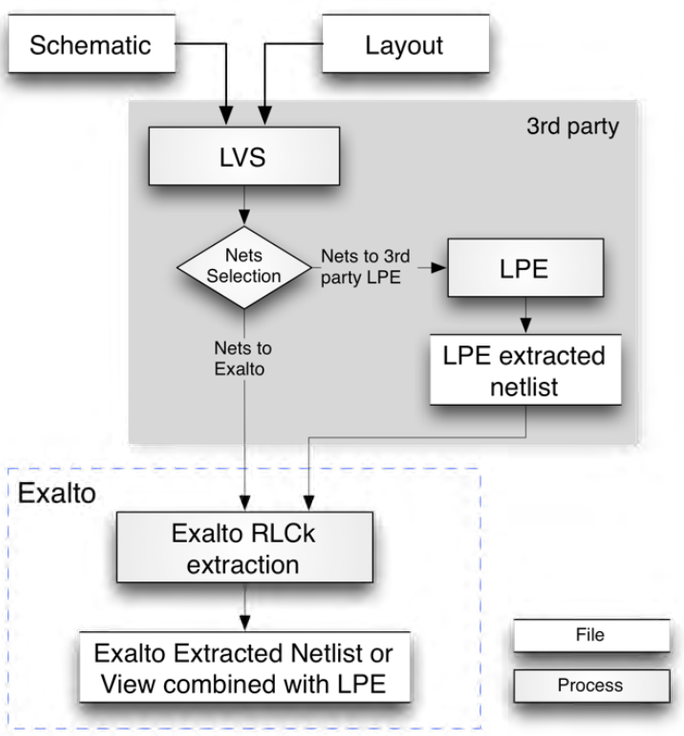

Figure 7. Integration of Exalto in the post-layout physical verification flow

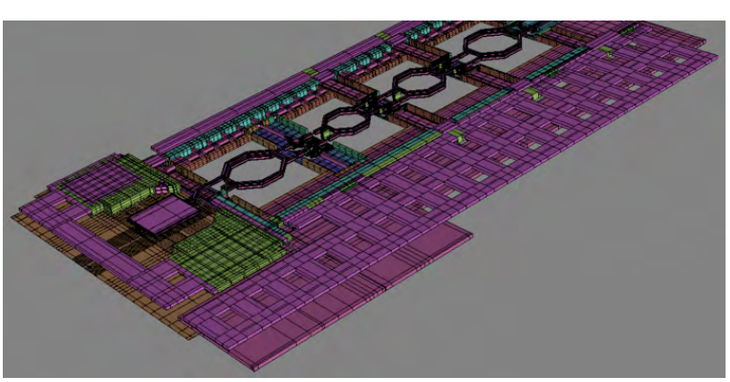

Figure 8. Low-noise amplifier (LNA) block meshed by Exalto

Accelerate Circuit Simulation Using the Most Appropriate Model Output from Exalto

Exalto generates passive, causal models in S-parameter format (for AC, harmonic-balance, and SP analyses) and rational function model (RFM) format suitable for transient, shooting, and noise analyses. Circuit simulation is no longer a challenge with the automation and variety of model formats of Exalto.

Compatible with All IC Design Platforms and Post-layout Physical Verification Flows

Exalto interfaces seamlessly with all leading custom IC design and post-layout physical verification platforms. The database of the parasitic extraction phase is an input for Exalto, while its output is an electromagnetic model for the electromagnetically critical part of your circuit. This model is automatically annotated to the output of the parasitic extraction tool so you can swiftly proceed to post-layout circuit simulation without manual effort.

A Fundamental Component of the Ansys On-chip Electromagnetic Simulation Workflow

Exalto is a key back-end component of a complete electromagnetic-aware design methodology that helps you sign off your high-frequency RFICs and digital SoCs with efficiency and confidence. Exalto massively accelerates the signoff phase with the widest coverage of electromagnetic parasitics and unique electromagnetic crosstalk prediction. The boost in productivity and signoff fidelity saves multiple days in design schedules when pressure peaks, time is most valuable, and the tapeout deadline is fast approaching.

ANSYS, Inc.
www.ansys.com
ansysinfo@ansys.com
866.267.9724